Energy Conversion
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공학박사 학위논문

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SWITCH-MATRIX ACTIVE EQUALIZATION STRATEGIES FOR MODULAR BATTERY ENERGY STORAGE SYSTEM

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Switch-Matrix Active Equalization Strategies for Modular Battery Energy Storage System

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This dissertation is submitted for the degree of
Doctor of Philosophy

University of Ulsan January 2023

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December 2022

I would like to dedicate this thesis to my loving parents who taught me that it is never too late to pursue your dreams, my Professor who always encourages and advices, and my wife who always there for me.

Declaration

I hereby declare that except where specific references are made to the work of others, the contents of this dissertation are original and have not been submitted in whole or in part for consideration for any other degree or qualification in this, or any other university. This dissertation is my own work and contains nothing which is the outcome of works done in collaboration with others, except as specified in the text and Acknowledgements.

Phuong-Ha La

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Abstract

The battery system plays an important role in renewable energy systems and electric vehicles. Since the battery system consists of multiple series-connected cells, over-charging or over-discharging can occur due to the heterogeneous characteristics of the cells. Thus, an effective equalizer is essential to maintain the cells' homogeneous performance, and thus extend their lifespan. Energy regenerative equalization systems provide different advantages in terms of capacity, speed, and efficiency. However, their performance depends on the initial energy distribution of the cells. On the other hand, there is no unified assessment method to compare the performances of equalizers. This thesis deals with the performance, effectiveness, and flexibility of the modular battery system. The main purpose of the research in this thesis is to develop a modular structure of the equalizer which can mitigate the inconsistency between cells and modules.

Firstly, a switch-matrix capacitor equalizer (SMC-E) is proposed for transferring energy between two cells directly. With the switch-matrix structure, a single capacitor is needed, thereby reducing the size of the equalizer. In order to achieve the shortest equalization time, an optimal pairing algorithm is introduced. The equalization process is divided into the scanning step and the pattern-holding step. Because the voltage deviation between two cells in the different pairs of cells is heterogeneous, their balancing currents are uneven. By scanning all possible balancing currents from all cell pairs, the optimal equalization pattern can be obtained, which has the highest balancing current. It is observed that only the pair of the highest voltage cell and the lowest voltage cell can have the highest compensating current. Thus, the optimal equalization pattern is the shortest way of transferring energy between the cells. The optimal equalization pattern is maintained for a period, T_h, before another current scanning step is activated. The optimal equalization pattern changes dynamically during the equalization process as the cell voltages change. By repeating the equalization

cycle, the energy is transferred between the cells as fast as possible. In addition, design instructions for operational and circuit parameters are provided. The hardware experimental results of the equalization verified the performance of the SMC-E in terms of equalization capability, speed, and stability. The cell-inconsistency is mitigated in all test scenarios, even if the energy distribution of the cells is different.

For a fair performance comparison for different equalizers in a short period of time, a simulation method based on a unified average model (UA-model) is proposed. By counting the amount of charge that flows out and into the cells, the equalization process of two-cells can be emulated by the UA-model. Since switching elements are suppressed in circuits, simulation based on the UA-model can be performed with a large sampling time, thus reducing the overall simulation time. In comparison with the RTSS simulation, the operational profiles of the UA and RTSS models have a homogeneous characteristics. The simulation method based on the UA-model has advantages as a platform of evaluation to fairly compare the performances of equalizers. The different equalizer topologies and designs can be tested under different initial test scenarios within a short period. Therefore, the design of the SMC-E may be evaluated and optimized.

The SMC-E can overcome the impact of initial energy distribution dependency, but the equalization time becomes longer as the number of cells increases. Thus, the fundamental analysis of equalizer performance at cell count is provided. To reduce equalization time, the modular structure of the SMC-E is available for both serial and parallel connected modules. In series-connected modules, the hybrid strategy is proposed to inherit the benefits of SMC-E, where several SMC-E units are activated at the same time. Once the cell voltages inside each module are equalized, the module equalization function is triggered to balance the module voltages. After two separate processes, the voltages of all cells are equalized in a small gap. The RTSS test results show a 13.5% shorter equalization time than the conventional method, where a single SMC-E is implemented for the whole cell string.

In addition, the same modular SMC-E design is applied to parallel-connected battery modules. In the parallel connection, the uneven distribution of current between the branches and the inrush current during the hot swap process are serious problems. Thus, two equalization strategies are proposed for SMC-E to address them in IDLE and non-IDLE modes. In IDLE mode, the modules are balanced by the same energy exchange scheme as

the modules connected in series. On the other hand, the energy levels of the modules are balanced during the charging or discharging processes by the current distribution scheme. Based on the test results on RTSS, the modules are equalized in the 4.82% SOC difference in the IDLE mode without the inrush current of the self-balancing effect. In addition, the modules can be equalized within 1% SOC difference in the charging and the discharging processes by the current distribution scheme. Thus, all modules are fully charged or fully discharged at the same time. The inrush current during the hot swap process is also mitigated since the branch currents can be adjusted by the SMC-E and the current distribution scheme.

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Chapter 1

Introduction

To deal with the shortage of fossil fuels, transport is progressively electrified [1]. Energy storage systems (ESS) using battery take an important role in the renewable energy system and EVs, where the battery pack is the main power source in the EV or the emerging storage system for the grid-tied energy storage system. In terms of the manufacturing and operating costs, the battery system takes over 50% portions of the annual cost of the energy storage system [2]. Thus, the battery system requires an efficient battery management system (BMS) to ensure a high performance and lifetime.

Since the battery pack consists of multiple series and parallel connected cells, the dissimilar performance of the cells is inevitable [3–5]. This chapter describes the common configurations of the cells in the ESS and the impact of cell-inconsistency on their performance in Section 1.1 and Section 1.2. From Section 1.3 to Section 1.5, an overview of the battery management system is reviewed and summarized. In addition, the performance indices and the level of equalization for the battery equalizer are introduced. Finally, the disadvantages and the

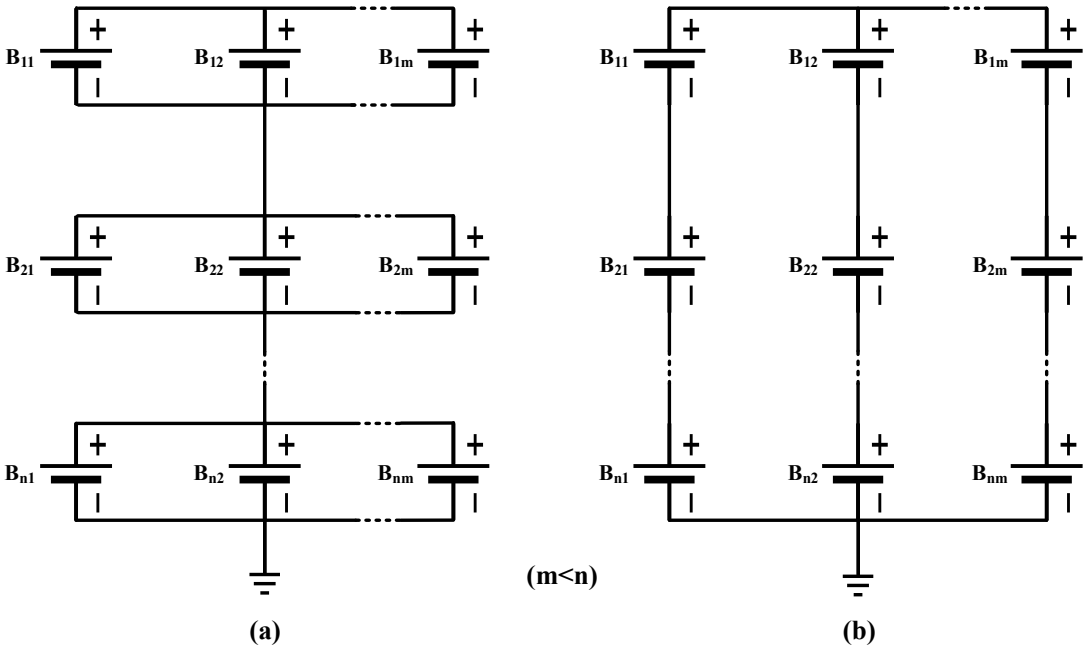


Fig. 1.1 Battery configuration in ESS: (a) nSmP configuration; (b) nPmS configuration.

problem of the conventional equalizers are identified, which highlights the research motivation for this thesis.

1.1 Battery Configuration in EV and BESS

In general, the battery cells are assembled to form a group or brick. Next, the groups or bricks are connected in series to form a module. Furthermore, the modules are connected in series to increase the operating voltage [6]. For illustrative purposes, two common configurations of the battery cells are shown in Fig. 1.1. The nPmS configuration in Fig. 1.1(a) is more popular in EV due to its cost-effectiveness. Since the characteristic of the cells is screened before the assembly, the similar characteristic cells are connected in parallel to utilize the self-balancing effect. Thus, only one BMS is required for the whole system in nSmP configuration while m BMS are needed in mPnS configuration. For example, the battery pack on the EV from

(a) (b)

Fig. 1.2 Example of cell configuration in EV: (a) Pouch type; (b) Cylindrical type.

Hyundai company consists of 10 modules configured by 20S3P pouch-type cells as Fig. 1.2(a). On the other hand, the battery pack on the EV of Tesla company divides the pack into 4 modules. The battery module consist of 24 bricks (groups), while a brick has 46 cells [7]. To be cost-effective, thousands of cylindrical cells are packed as in Fig. 1.2(b). The large-capacity battery system can be formed with a less parallel cell-inconsistency effect by paralleling the small-capacity cells. It is because the impact of the characteristic mismatching is partially dominated by the number of parallel connections. Besides, the manufacturing cost is more efficient since the labor cost can be divided into a large quantity of cells.

In addition, the configuration of nPmS in Fig. 1.1(b) is more suitable for the large-scale ESS in the grid-tied application, which requires a large-capacity and high-voltage battery system. However, compared with the nSmP configuration, the nPmS configuration requires more BMS, which increases the cost since individual cells can be monitored and controlled to achieve the optimal performance and efficiency of the battery system. In nPmS configuration, the battery racks are connected in parallel through the relays. The power distribution between the racks depends on their operational conditions such as state-of-charge (SOC), impedance, and state-of-health (SOH).

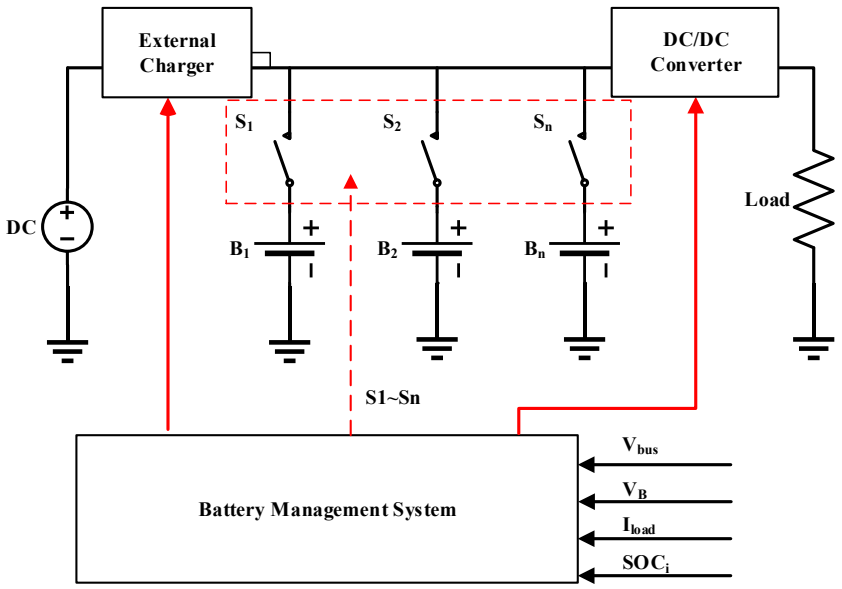


Fig. 1.3 Battery configuration in telecommunication and datacenter applications.

By the same token, low-voltage battery modules are connected in parallel to enlarge the system capacity as in Fig. 1.3. The relays or the contactors are utilized to dock the battery modules to the DC bus based on their state conditions. To achieve the highest operation effectiveness, the scheduling algorithms are applied to fully utilize the available capacity of the battery modules. Besides, the cell-inconsistency can cause an inrush current in the hot-swap application, where the battery modules are replaced and are suddenly docked to the DC bus. The effect of the cell-inconsistency will be deeply analyzed in Section 1.2 of this chapter and a modular equalization strategy is proposed in Chapter 4 to mitigate it.

In all configurations, the system performance is strongly dependent on the cell uniformity. The cell inconsistency can lead the battery system to over-charging, under-charging, or overload when the characteristics of the cells are different in terms of capacity, impedance, and dynamic response. Performance mismatch is inevitable due to the material tolerance in the manufacturing process. Although the characteristic of the cells is screened before the

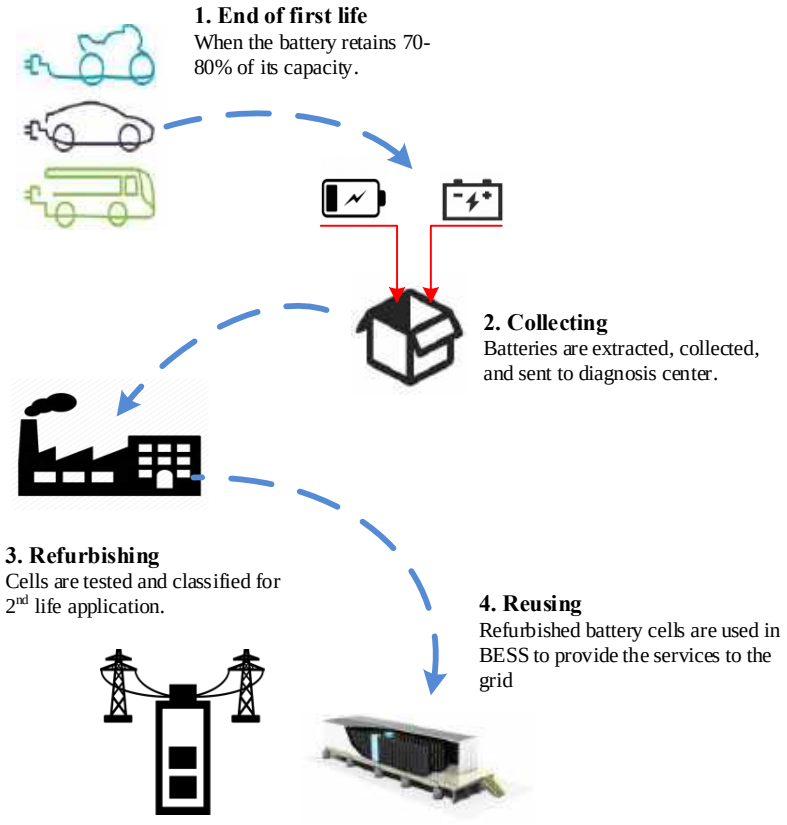


Fig. 1.4 Life cycle and seconds-life battery concept.

assembly [8, 9], the performance consistency is only guaranteed in the first few operating cycles. Since the aging of the cells occurs under different patterns, the impact of the cell-inconsistency becomes more serious. Thus, the BMS is required to monitor the performance of the cells and protect the system in case of failure.

In another story, the significant growth of the EV fleet on the road also raises concerns about how to deal with the retired battery packs from EVs. According to the United States Advanced Batteries Consortium, the EV battery pack should be replaced when its capacity is reduced to 70 % $\sim$ 80 % [10] to ensure the operation range of EVs. The predicted retired battery packs can reach 6 million packs per year [11] or 100-200 GWh [1] by 2030. The retired

battery packs can become a significant burden to the recycling industry. Although battery recycling is paid the attention to [12–14], the cost of labor is too high which prevents its practical feasibility. In addition, the recycling efficiency of rare metals is not high, reducing interest in the industry.

In view of the economic value, almost 80 % capacity of the retired battery pack is remaining that can be reused for other purposes such as ESS for the power grid, UPS applications, or small-scale electric vehicles. The reusing purpose is assessed and verified to be more beneficial in the view of economic and environment [15–19], which is usually called second-life battery (SLB) application. The concept of the SLB application is illustrated in Fig. 1.4, where the retired battery packs are returned to the manufacturer through the after-service and repair system. Next, the manufacturer detaches the cells inside the packs and classify them based on their state conditions. In some cases, the whole retired battery packs are sent to the market directly without the detachment to reduce the labor cost. Finally, the refurbished cells/packs are assembled again to provide the services to the ESS application. It should be noted that the cell characteristics becomes further mismatch compared to the new cells. Cell-inconsistency will be discussed further in Section 1.2.

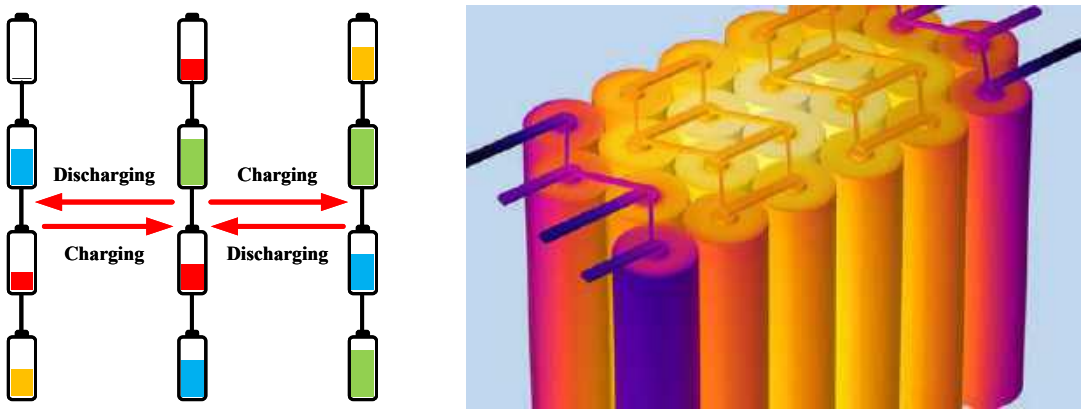


Fig. 1.5 Cell-inconsistency in series connection: (a) Mechanism of the over-charging and under-charging issue; (b) Thermal runaway effect of the cells.

1.2 Cell-Inconsistency and its Impact on the Performance of the Cells

The characteristic heterogeneity, which is called cell-inconsistency, between the cells can lead the entire battery system to be overcharged or undercharged. The cell-inconsistency appears in different patterns in the series and parallel configuration. In this section, the impact of the cell-inconsistency will be analyzed for both series and parallel connections of the battery cells.

1.2.1 Cell-Inconsistency in Series Connection

The cell-inconsistency in the series connection can be vividly demonstrated in Fig. 1.5, where the energy level of the cells is uneven due to the non-uniform aging conditions. Since the operating current of the cells in a series connection is the same, the changing amount of charge in the cell is also similar. Thus, some cells can be fully charged before the other cells, or some cells can be fully discharged before the other cells. If the charging/discharging

process is monitored by the terminal voltage of the entire pack, the system cannot recognize the cell-inconsistency. If the charging/discharging process is continuously executed, the high-voltage cell group can be led to overcharging and lowest-voltage cell group can be led to under-discharging.

The mechanism of overcharging is described in [20–22], where the internal structure of the cell breaks down a chain reaction. Firstly, the solid electrolyte interface (SEI) is formed during the cell operation, which reduces the available capacity and increases the cell impedance. Since overcharging/under-discharging occurs, the SEI layer is decomposed. The metal in the collector is dissolved into an ion, and thus, the separator is shorted through when the metal-ions are compound. Thus, the cell has an internal shorted, which will release a lot of energy through the heat. Next, the heat is continuously accumulates inside the cell and also affects the temperature of the adjacent cells in the pack. When the pressure inside the cell is too high, the cell can be deformed and explored [23, 24]. Heat and fire from the accident can start a fire in the adjacent cells and consequently in the entire pack as a chain reaction. That's why individual monitoring of the cells is required in the BMS to stop the charging/discharging process when a cell voltage reaches the maximum/minimum thresholds. Even if the cells are not caught in fire, the available capacity of the battery pack can be reduced, and thus, the lifetime of the battery system becomes shorter. It means that if the cell-inconsistency is not mitigated, the battery system must be replaced sooner than expected. In this thesis, the equalization strategies for the modular BESS are proposed in Chapters 2 and 4 to mitigate the cell-inconsistency in the series connection.

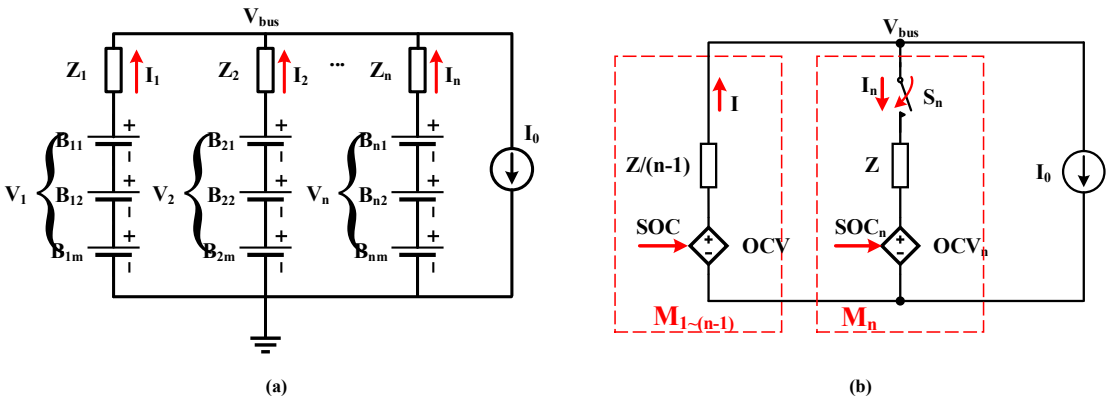


Fig. 1.6 Cell-inconsistency in parallel connection: (a) Equivalent circuit of parallel connected battery module; (b) Equivalent circuit of hot-swap operation.

1.2.2 Cell-Inconsistency in Parallel Connection

The parallel connection of the battery modules is popular for telecommunication and data-center applications. Although the characteristics of the modules are initially screened and made similar, the operation current soon becomes dissimilar between the branches due to the degradation of the cells. Even when the battery system is in idle mode, the circulating current always exists between the parallel modules by nature. The equivalent circuit in Fig. 1.6(a) illustrates the impact of the cell-inconsistency on the performance of the battery modules. In this model, a module is modeled by a voltage source and a series impedance.

Assume that the parallel battery modules are operated under a constant current, I_0, and the currents in the branches are expressed as

$$\begin{aligned} Z_1 I_1 - Z_2 I_2 &= V_1 - V_2 \\ Z_1 I_1 - Z_3 I_3 &= V_1 - V_3 \\ &... \\ Z_1 I_1 - Z_n I_n &= V_1 - V_n \\ I_1 + I_2 + I_3 + ... + I_n &= I_0, \end{aligned} \tag{1.1}$$

where $V_1,\ V_2, ...,\ V_n$ are the open-circuit-voltage of the battery modules, respectively; $Z_1,\ Z_2, ...,\ Z_n$ is the internal impedance of the modules; $I_1,\ I_2, ...,\ I_n$ is the operation currents of the branches. For an illustrative purpose, the operation currents of three parallel battery modules are calculated by

$$\begin{aligned} I_1 &= \frac{I_0 Z_2 Z_3}{Z_2(Z_1+Z_3)+Z_1 Z_3} + \frac{V_1(Z_2+Z_3) - V_2 Z_3 - V_3 Z_2}{Z_2(Z_1+Z_3)+Z_1 Z_3}, \\ I_2 &= \frac{I_0 Z_1 Z_3}{Z_1(Z_2+Z_3)+Z_2 Z_3} + \frac{V_2(Z_1+Z_3) - V_1 Z_3 - V_3 Z_1}{Z_1(Z_2+Z_3)+Z_2 Z_3}, \\ I_3 &= \frac{I_0 Z_1 Z_2}{Z_2(Z_1+Z_3)+Z_1 Z_3} + \frac{V_3(Z_1+Z_3) - V_1 Z_2 - V_2 Z_1}{Z_2(Z_1+Z_3)+Z_1 Z_3}. \end{aligned} \tag{1.2}$$

It is observed from (1.2) that the operating current of the parallel branches is strongly dependent on the battery impedance and OCV. Since the operating currents of the branches are uneven, one or more battery modules must be operated by a higher current that may can lead to an overload condition. Thus, there is always a battery group that has a higher temperature than the others due to the inconsistency. By the same token of over-

charging/under-discharging mentioned in Section 1.2.1, the short-circuit occurred in a branch may short the entire parallel connection. Hence, the damage caused by cell-inconsistency in a parallel connection can be more serious than that in a series connection.

On the other hand, the battery system of telecommunication and data-center system should not be shut down, even during maintenance. Thus, hot-swap maintenance is utilized to replace the battery modules will be very useful. However, the mismatch between the newly replaced module and the existing modules is sometimes significant. In this case, a pre-charging circuit consisting of the pre-charge switches and resistors [25] is not sufficient to suppress the high inrush current [26]. The equivalent circuit in Fig. 1.6(b) represents the mechanism of the inrush current in the hot-swap operation. The sharing current of the branches is corrected with equation (1.1), where the existing modules have to be discharged by the high current to charge the replaced module. It is observed that the inrush current is maintained and uncontrollable as long as the energy levels of the parallel branches are different from each other. Therefore, the cell-inconsistency in parallel connection should be carefully handled to ensure the safety of the battery system.

1.2.3 Hardware Test Datasets for Cell-inconsistency

To discuss the issue of cell-inconsistency in more detail, it is necessary to access the aging pattern of the cells. For this purpose, multiple cell samples are cycled in the same conditions, which is set up as in Fig. 1.7. The battery cells are put into a heat chamber to emulate the ambient temperature of the battery pack. Next, the cells are cycled under different test sequences to obtain the operating parameters or the state condition of the cells during the cycle test. According to the tests, various open source datasets are provided by the research

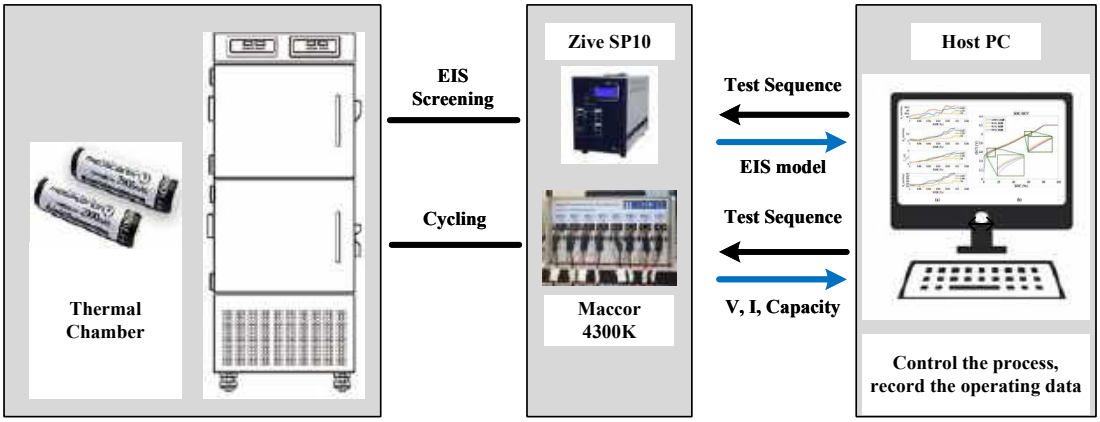


Fig. 1.7 Experimental setup for the aging assessment.

community such as NASA [27, 28], Oxford [29], Berkeley [30], MIT [31], and more datasets information is summarized in [32].

In [33], multiple samples of Kokam SLPB533459H4-740mAh are cycled by 1 C-rate in 40-degree Celsius ambient. The capacity of the cells is recorded every 100 cycles and the capacity degradation of 6 cells is illustrated in Fig. 1.8(a). It is observed that the capacities become dissimilar as the number of cycles increases. Meanwhile, the pattern of cell aging is dissimilar even when the operating conditions are the same. The different aging pattern occurs because of the material tolerance during the manufacturing process.

In fact, the cell-inconsistency is arbitrary and there is no common pattern in various configurations and applications. In [34], the SOH levels of 34 retired battery cells (3.7V-32Ah) are assessed after more than 2-years of actual operations. The capacity of the cells normally shows the different aging patterns. Most of the cells have 80% to 95% SOH levels, while some cells are strongly degraded at 60 %. Thus, the cell-inconsistency becomes more serious during the operation of the battery pack, especially in second-life battery applications.

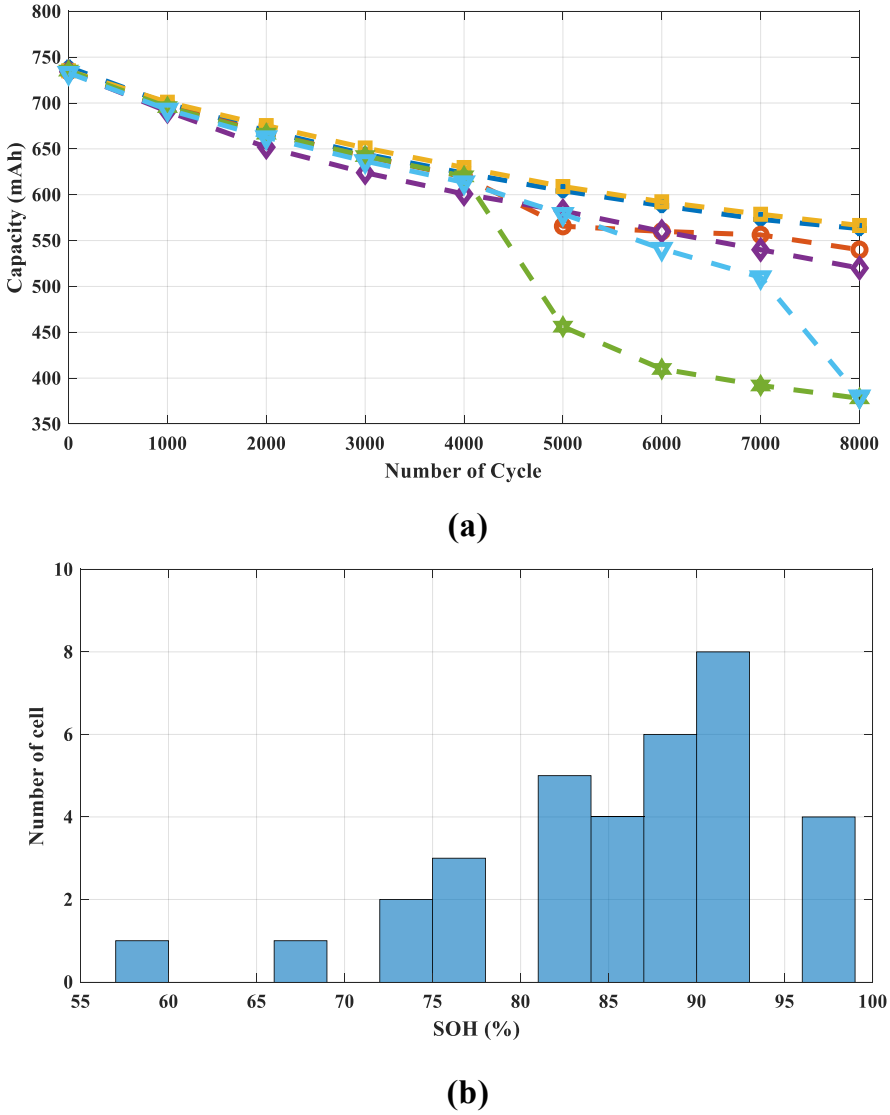


Fig. 1.8 Aging pattern and its probability: (a) Capacity vs. number of cycles; (b) SOH distribution of 34 retired battery modules in EV.

Stochastic and statistical approaches are applied to predict the characteristic difference between the cells in order to mitigate the cell-inconsistency in a second-life battery application. In [35–37, 34], numerous retired battery cells are screened to assess the characteristic distribution. For the illustrative purpose, the distribution in terms of available capacity and internal resistance (DCIR) for 50,000 battery cells (18650-3.7V/3Ah-20$m\Omega$) are presented

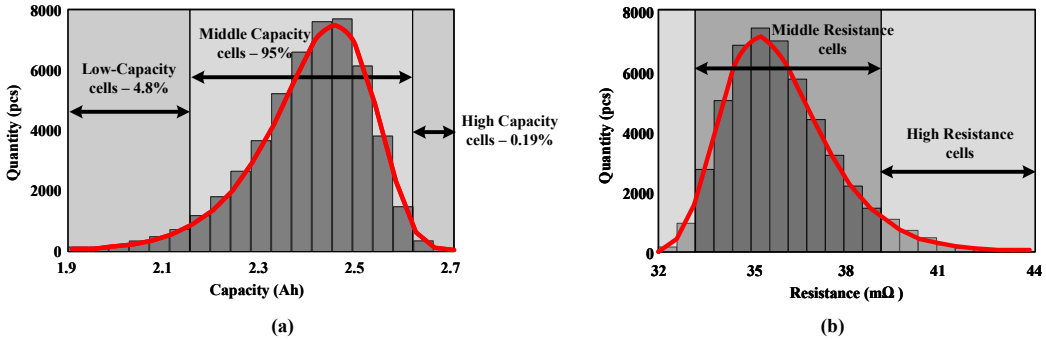


Fig. 1.9 Distribution illustration for 50,000 Li-ion 18650 cells (3.7V-3Ah-20$m\Omega$): (a) Available Capacity; (b) DC resistance.

in Fig. 1.9 (a). In view of the capacity, the low-capacity or high-capacity cells take a small portion of the distribution. However, the mid-capacity cells, which have a 20% difference of capacity, take the majority of the distribution (95%).

Similarly, the distribution of the DCIR of the cells is shown in Fig. 1.9(b). For capacity and DCIR, the distribution can be represented by a Weibull distribution. Based on the distribution model, the state of individual cells can be approximated from the state of the battery pack, thus, improving the safety of the battery system. In fact, homogeneity of cell performance can be ensured by limiting the acceptable range of the capacity or DCIR difference. However, the number of extruded cells becomes higher and requires a higher labor burden to recycle them.

To recapitulate the impact of the cell-inconsistency on the battery system, the charging and discharging processes of a 3S4P battery pack are accessed by a simulation platform. In the battery pack, the mismatch of the capacity and DCIR of the cells is set to 20% randomly. In addition, the pack is charged by the CC-CV 12.6V-10A method and is discharged by a CC 10A load. The current and SOC profiles of the cells are illustrated in Fig. 1.10, which show an unequal current sharing between the parallel branches. Consequently, the cells are

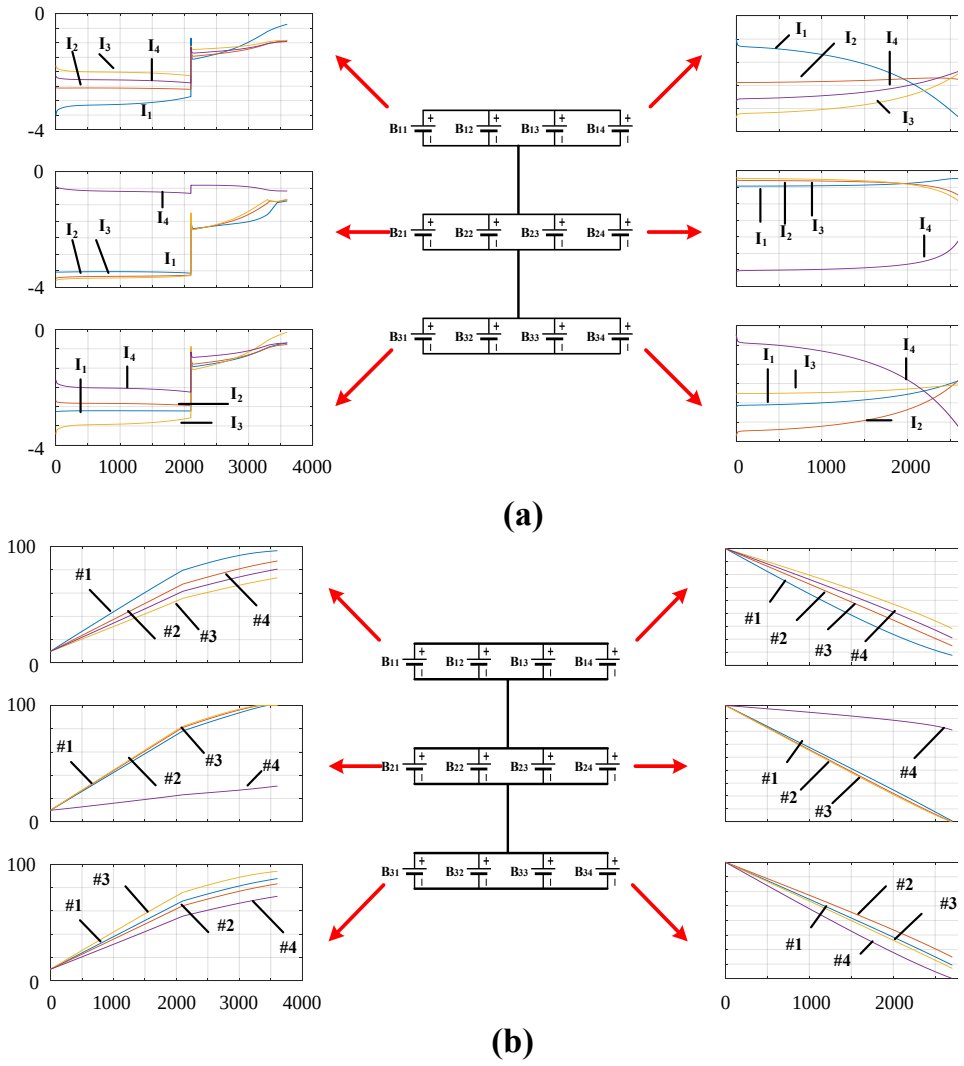


Fig. 1.10 Impact of the cell-inconsistency: (a) un-equal current sharing of the branches; (b) SOC mismatching during the operation.

not fully charged or fully discharged as Fig. 1.10(b), and thus, can cause the over-charging or under-discharging issue if the processes are not terminated. Thus, the battery equalizer is essential to mitigate the cell-inconsistency and improve the operational effectiveness of the entire system.

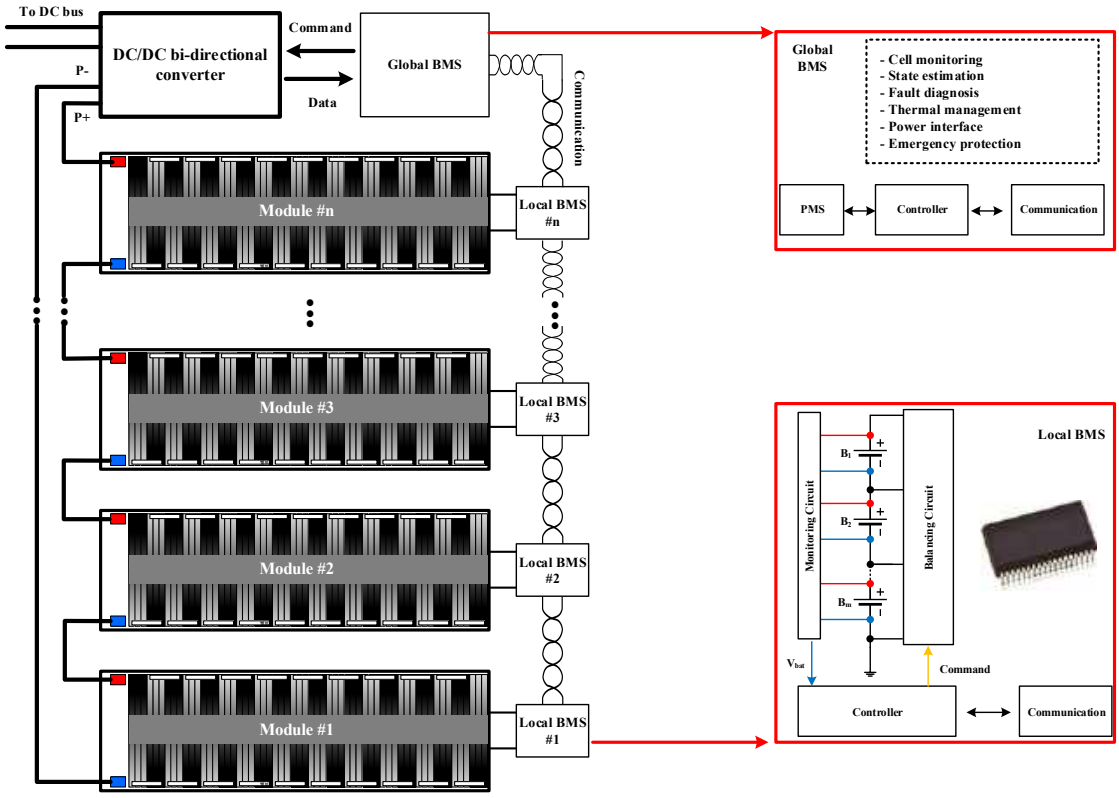


Fig. 1.11 Modular structure of the BMS in EV and BESS.

1.3 Overview of Battery Management System in EV and BESS

In EV and BESS, a battery pack is divided into multiple modules. For each module, a local BMS is used to monitor and balance the energy of the cells inside a module, as shown in Fig. 1.11. The local BMS consists of a battery monitoring circuit, a balancing circuit, a communication block, and a control block. Generally, the most part of the local BMS is integrated into a BMIC chip, which significantly reduces the volume and cost of the local BMS. A BMIC can monitor 12 or 16 series-connected battery cells and a few examples of

Table 1.1 COMPARISON OF BMIC FEATURES.

Manufacturer	**Model**	**No. of Channel**	**Balancing**	**Communication**	**Measuring error**	**Temp. sensing channel**
Analog Devices	**LTC6804**	12	Passive	Daisy Chain Iso-SPI	1.2mV	2
Analog Devices	**LTC6811**	12	Passive & Active	Daisy Chain Iso-SPI	1.2mV	2
Infineon	**LLE9012DQU**	12	Passive	Iso-UART	78mV	5
STMicroelectronics	**L996963E**	14	Passive	Iso-UART	2mV	7
Texas Instruments	**bq76PL455A-Q1**	16	Passive & Active	Iso-UART	3mV	8
Maxim Integrated	**MAX17823B**	12	Passive	Daisy Chain Iso-UART	5mV	2

commercial BMICs are summarized in Table 1.1 for a comparison. According to the number of series-connected cells in the modules, the number of BMICs in the local BMS is determined.

Since the local BMSs are linked by the Daisy Chain ISO-communication, the global BMS can read all operating parameters of the cells such as voltage and temperature. In the global BMS, the state conditions of the modules or the pack are estimated to ensure safety and the cell voltage and temperature are continuously monitored for failure diagnosis. The global BMS can trigger the balancing function in the individual local BMS when the cell-inconsistency inside a module is detected. While the equalization between the cells can be ensured, module-to-module balancing is not guaranteed. In addition, the global BMS can trigger the protection function on the power management system (PMS), when fault conditions are detected on a module.

1.4 Battery Equalizer

As mentioned, the equalizer is utilized to balance the energy level of the cells in the series string, and thus, to resolve the impact of cell-inconsistency issues. Various balancing techniques with different topological configurations have been developed and can be classified into two groups: dissipative energy scheme and regenerative energy scheme as shown in Table 1.2.

Table 1.2 CLASSIFICATION OF BATTERY EQUALIZERS

Ref.	Structure	Equalization Scheme	Target Objects	Control Technique
[38],[39]	Switched Resistor	Dissipative	Individual cell	Governed
[40]	Shunt MOSFET	Dissipative	Individual cell	Governed
[41]	Multiple Converters	Regenerative	Individual cell	Governed
[42]	Switch-matrix and Converter	Regenerative	Direct pack to cell	Governed
[43],[44], [45]	Multi-winding or Multiple Transformer	Regenerative	Any-cell to any-cell	Autonomous
[46], [47]	Switched Inductor	Regenerative	Adjacent cells	Autonomous
[48]	Switch-matrix and Inductor	Regenerative	Direct any-cell to any-cell	Governed
[49]	Switched Capacitor-Classical Structure	Regenerative	Adjacent cells	Autonomous
[50]	Switched Capacitor-Double-tiered Structure	Regenerative	Adjacent cells	Autonomous
[51]	Switched Capacitor-Chain Structure	Regenerative	Adjacent cells	Autonomous
[52]	Switched Capacitor-Star Structure	Regenerative	Any-cell to any-cell	Autonomous
[53]	Switched Capacitor-Reconfiguration	Regenerative	Adjacent cells	Autonomous
[54], [55], [56]	Switched Resonance Structure	Regenerative	Any-cell to any-cell	Autonomous

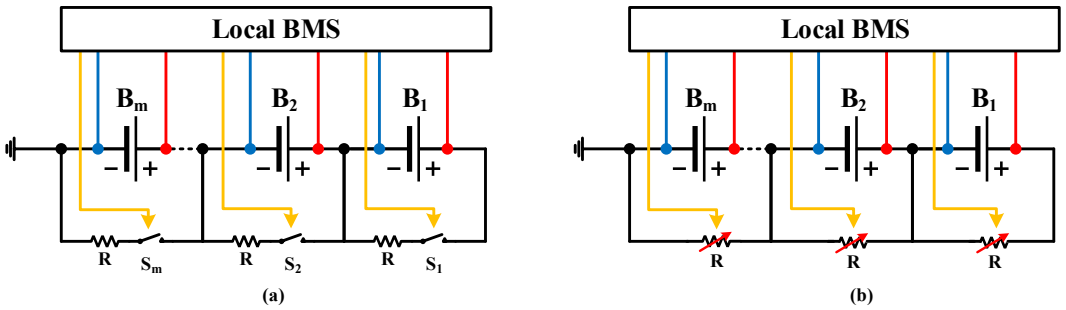


Fig. 1.12 Dissipative energy scheme: (a) switched-resistor; (b) variable resistance using MOSFET.

1.4.1 Dissipative Energy Schemes

The dissipative energy scheme has been widely accepted by the industry because of its simplicity, simple control, and individual cell processing. Most dissipative energy schemes are implemented by either switched resistor in Fig. 1.12(a) [38, 39] or MOSFET in Fig. 1.12(b) [40]. By turning on the switch of the balancing circuit as in Fig. 1.12(a), the high voltage cells are discharged by their resistor until the energy level of all cells is equalized. The switches are easily integrated into the BMIC and the cell is discharged by the external resistor. However, its energy efficiency is low due to the dissipative energy scheme. In addition, a cooling

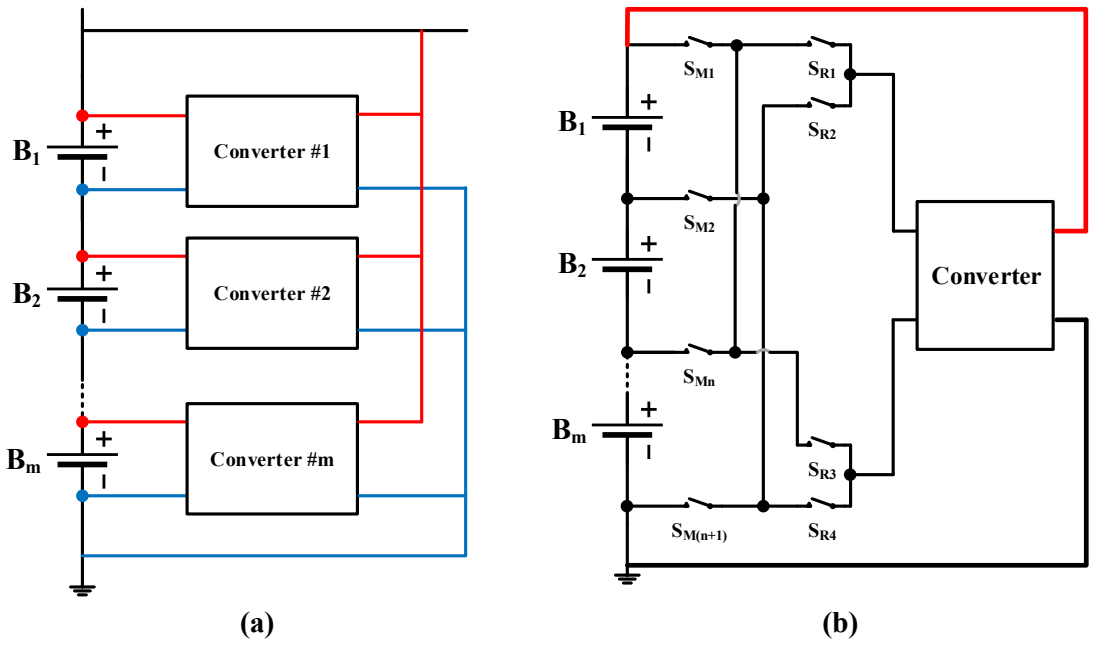


Fig. 1.13 Regenerative energy scheme group - Converter & Transformer type: (a) Individual converter; (b) Switch-matrix converter.

system is essential when the balancing current is high for a high equalization speed. Since the passive balancing method is integrated into the BMIC, the balancing current must be limited to prevent the overheating issue for the IC. Thus, the equalization speed of the BMIC based BMS is relatively low. On the other hand, the switch and resistor are replaced by a semiconductor circuit, which serves as a variable resistor as in Fig. 1.12(b). By controlling the gating voltage, V_{gs}, the discharging current through the circuit can be regulated. Although energy loss is reduced, it raises a safety concern when the cells can be shorted by the switch and cause an accident. In addition, the dissipative energy scheme can waste the lifetime of the cells.

1.4.2 Regenerative Energy Schemes I - Converter Type

To improve the battery utilization, the converter based methods are utilized to transfer energy between the cells. In Fig. 1.13(a), multiple isolated converters are used to exchange energy between the cell and the entire series string individually. Therefore, the high equalization capability, speed, and efficiency can be achieved [41, 57]. However, the isolated converter is required to prevent the short circuit during the equalization process since the converter output grounds are connected together. In addition, a complex measuring and control system are required.

To save the space, a switch-matrix and a converter are used instead as shown in Fig. 1.13(b). By controlling the switch-matrix pattern, BMS can select a cell in the series string to perform the charging or discharging process [42]. Depending on the cell inconsistency, the switch-matrix pattern is changed alternately until the energy levels of the cells are equalized. The switch-matrix converter method can play a similar role to the individual converter method. However, the switch-matrix converter structure reduces the equalization speed because only one cell can be processed at a time.

Actually, the converters in Fig. 1.13(a) and 1.13(b) can be implemented either by the individual transformer [43, 44] and multi-winding transformer [45] as in Fig. 1.14(a) and (b). Depending on the voltage difference between the cells, the duty ratio of the switches is calculated to control the balancing current. The equalization operation is controlled by a complementary pair of PWM signals and the energy is transferred between the battery module and the cells autonomously. Although the volume is reduced, the number of windings in a transformer is limited due to the limited window size of the core. Thus, it is difficult to apply the multi-winding transformer for a large number of cells.

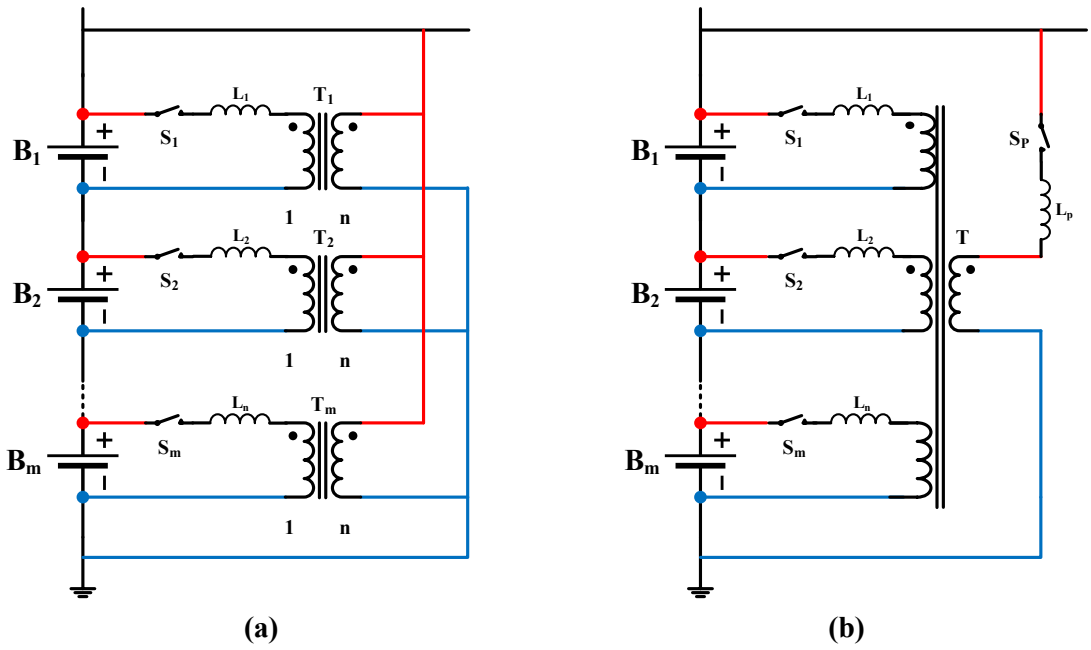


Fig. 1.14 Regenerative energy scheme group - Transformer type: (a) Individual transformer; (b) multi-winding transformer.

1.4.3 Regenerative Energy Schemes II - SET-E Types

The switched energy tank equalizer (SET-E) is a simplified version of the converter and transformer based methods. The most popular representation is the switched-inductor equalizer (SI-E), where an inductor serves as an energy carrier to exchange the energy level of two adjacent cells [46, 47]. To equalize the voltage of all cells, the cascading or hierarchical structures of the SI-E or the coupled-inductor are adopted [58, 59]. However, the volume and cost still hinder their practical feasibility.

In terms of energy density, the capacitor can achieve a significantly higher energy density with a smaller volume compared to the inductor [60] as in Fig. 1.16. Thus, the capacitor can replace the transformer or inductor as an energy tank in the equalizers for downsizing. Various topological configurations of the SC-E have been introduced in recent years with

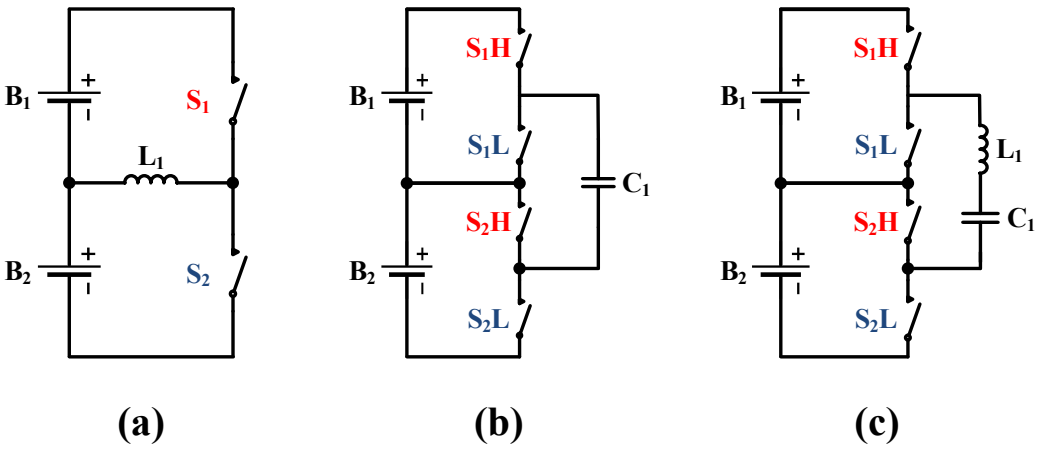


Fig. 1.15 Energy regenerative schemes II - SET-E types: (a) SI-E, (b) SC-E, (c) SR-E.

batch variants. In this thesis, the typical representatives of the capacitor based equalizer are including classical structure [49], double-tiered structure [50], chain structure [51], and star structure [52], respectively.

The SC-E type uses the same switching network structure, where two switches are attached to a cell. Next, the capacitor network is docked to the middle of the switches, where a capacitor is utilized to exchange the energy of 2 adjacent cells. By turning on and off the upper switches and the lower switches alternately, the capacitors are charged by the higher voltage cell in phase A, and the stored energy will be released to the lower voltage cell in another phase autonomously. Observed that the amplitude and direction of the balancing currents depend on the voltage difference between two cells, and thus, the balancing current gradually decreases as the balancing is achieved. In the classical structure, energy must be transferred through many intermediate steps if the highest voltage cell and lowest voltage cell are located far away. In the double-tiered SC-E, more capacitors are added to the capacitor network in order to increase the equalization speed, which can balance the energy of two adjacent groups consisting of two adjacent cells. By the same token, four switches and one

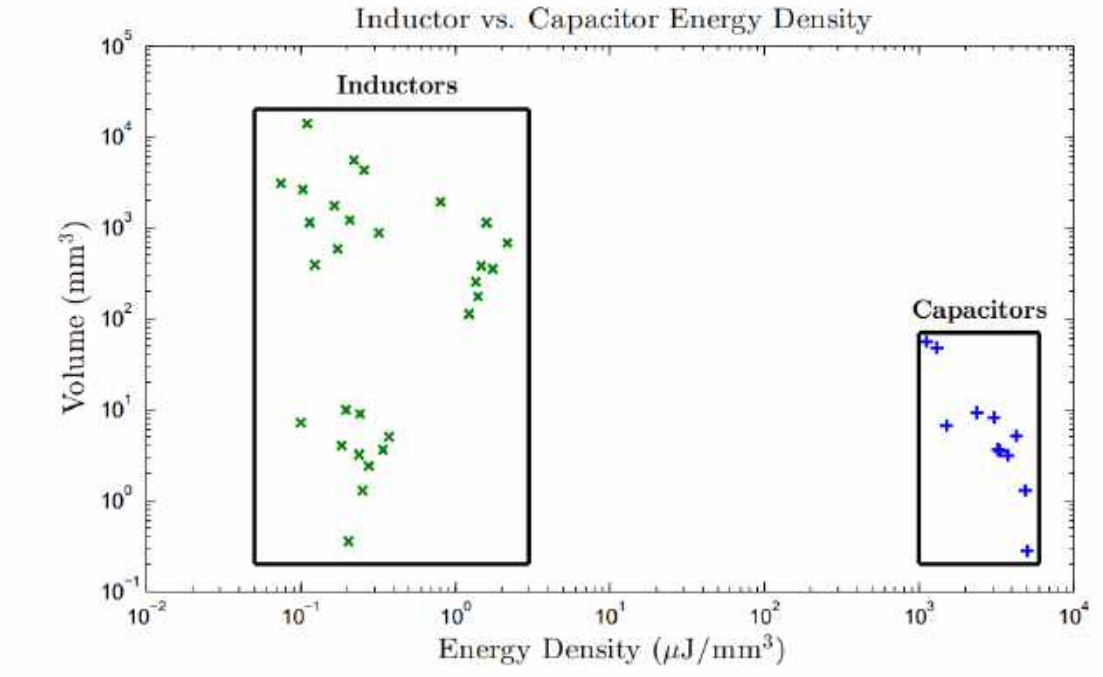


Fig. 1.16 Energy density comparison of inductor vs. capacitor.

capacitor are added to the chain structure of SC-E. Because the energy of the first and the last cells is exchanged through the additional circuit, the equivalent distance between the highest voltage cell and the lowest voltage cell is reduced to half. On the other hand, the star structure is introduced to reduce the number of capacitors in the equalizer. The star network of capacitors serves as a rotary, which can autonomously transfer energy from any-cell to any-cell. However, the number of balancing capacitance is reduced to half of the other methods reducing the balancing current.

Although the SC-E only requires a complementary PWM signal pair to autonomously process the equalization, the autonomously control strategy is also a critical disadvantage of the SC-E types. Since energy is only exchanged between two adjacent cells, more and more capacitors tiers should be added to increase the equalization speed. However, the additional energy tier indirectly increases the energy loss and the cost of the equalizer. Thus, the

resonant technology is applied to improve the performance of the SC-E type. By the same operating principle, an inductor is added in series with the balancing capacitor [56, 54, 55]. In the optimal design, the energy loss during the equalization process can be reduced. On the other hand, the balancing capacitance and resonant inductance are small in the resonant condition which reduces the size of the equalizer.

In summary, the generative energy schemes are more promising than the dissipative energy schemes for cell equalization in terms of energy efficiency and lifetime. Although the dissipative energy schemes are more popular in the industrial applications, the generative energy schemes will gradually replace the dissipative energy scheme, especially in the SL-BESS where a high-performance equalizer is required.

1.5 Battery State Estimation and Monitoring

In general, the cell characteristics are screened to sort cells in terms of available capacity and DCIR. In addition, the cell voltage, operating current, and temperature are continuously monitored by the local measurement circuits or BMICs. After that, the measured information is sent to the global BMS, where the aging and state conditions of the cells/modules are estimated. To assess the state conditions of the battery system, the SOC level, SOH level, and remaining useful lifetime (RUL) are specially considered. Various state estimation methods can be adopted for the battery system and can be classified into the Coulomb counting method, the model-based methods, and the data-driven methods [61].

The Coulomb counting methods estimate the amount of charge that flows into or out of the battery system during the operation based on the current measurement [62, 63]. The

initial capacity level of the battery system is stored for historical data and the capacity level of the battery system is calculated by

$$Q(t+\Delta T) \;=\; Q(t)+\int_{t}^{t+\Delta T} i(\tau)d\tau. \tag{1.3}$$

Hence, the SOC and SOH levels are presented as

$$\begin{aligned} SOC(t+\Delta T) &= \frac{Q(t+\Delta T)}{Q_{full}} \\ &= SOC(t)+\frac{\int_{t}^{t+\Delta T} i(\tau)d\tau}{Q_{full\_@t}}, \end{aligned} \tag{1.4}$$

$$SOH(t+\Delta T) = \frac{Q_{full\_@t}}{Q_{new}}, \tag{1.5}$$

where $Q_{full\_@t}$ and Q_{new} are the actual capacity of the battery at this current state and the design capacity of the battery. Because the operating current of the series cells is the same, the Coulomb counting can be applied for the entire battery pack or module with a pre-defined inconsistency distribution, mentioned in Section 1.2.3. However, the estimating accuracy is strongly dependent on the precision of the current sensor. Therefore, the model of the entire battery pack with consideration of cell-inconsistency is required to ensure the accuracy of the state estimation.

On the other hand, model-based estimations such as the Kalman filter estimator and their variant are good candidates to replace the Coulomb counting methods. Based on the measured cell voltage, operating current, and cell temperature, the predicted voltage and SOC can be estimated through the state space equations [64–68]. With a fast convergence feature, the model-based methods can achieve a high estimation accuracy as well as low

computation time. Thus, it is possible to apply the model-based estimations for individual cells. However, the high-precision state space model is required for each cell to ensure the estimation accuracy. Considering the cell-inconsistency and the different aging patterns, the state space equation of the estimator must be updated during the operation of the battery pack [69].

To mitigate the problem of the state space model accuracy in the model-based estimations, data-driven methods have been recently adopted. From the basic operating parameters such as cell voltage, operating current, and temperature, we can obtain the battery models, SOC level, or SOH level of the battery pack [70–73]. Nevertheless, a huge dataset must be used to train the estimation model, which requires a lot of computation resources. Thus, a high-speed computation machine is needed to execute the estimation. When it comes into the estimation for individual cells in the series string, the computation will become far more complex.

1.6 Performance Indices for Battery Equalizer

In order to have a unified performance assessment for various battery equalizers, various evaluation criteria are presented in Fig. 1.17. Every criterion can be prioritized based on the requirement of the applications. From an academic perspective, the equalization capability, the equalization speed, and the performance stability will have a higher order of priority than the others. Vice versa, the industrial field is more inclined to consider the cost and volume of the equalizer. The definition of each evaluation criterion is described as follows:

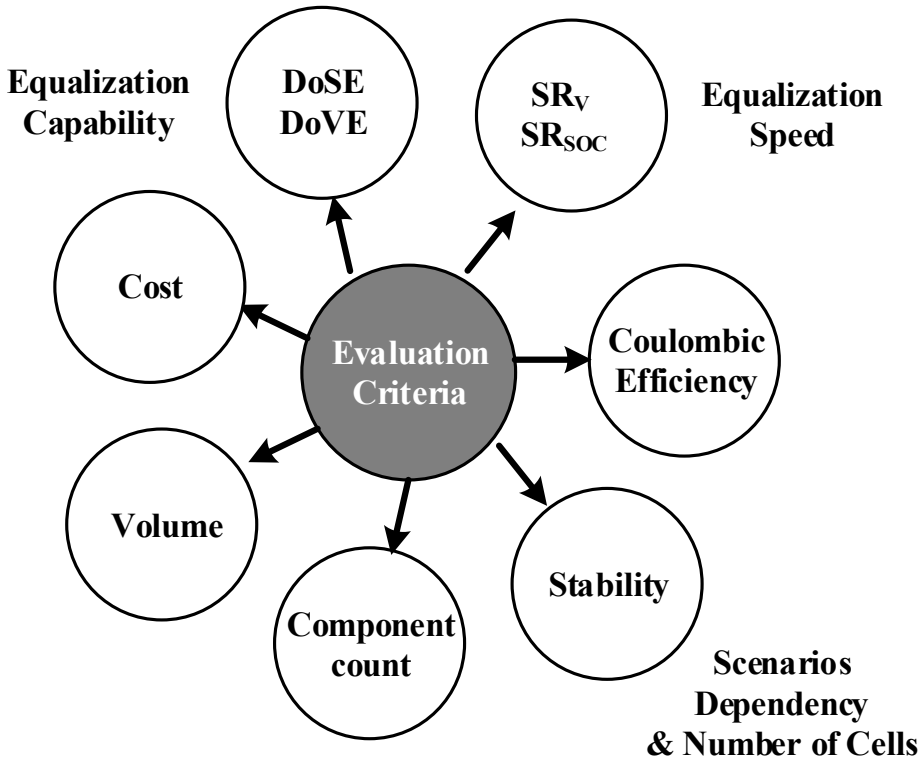


Fig. 1.17 Various performance indices for the equalizer.

• **Equalization capability** is assessed based on the degree of SOC estimation (DoSE) and degree of voltage estimation (DoVE). The DoSE and DoVE are defined by

$$DoSE = \frac{\Delta SOC_{initial} - \Delta SOC_{final}}{\Delta SOC_{initial}} \tag{1.6}$$

and

$$DoVE = \frac{\Delta V_{initial} - \Delta V_{final}}{\Delta V_{initial}}, \tag{1.7}$$

where $\Delta SOC_{initial}$ and $\Delta V_{initial}$ are the initial SOC deviation and the initial voltage deviation between the cells before the equalization; and ΔSOC_{final} and ΔV_{final} are the deviation

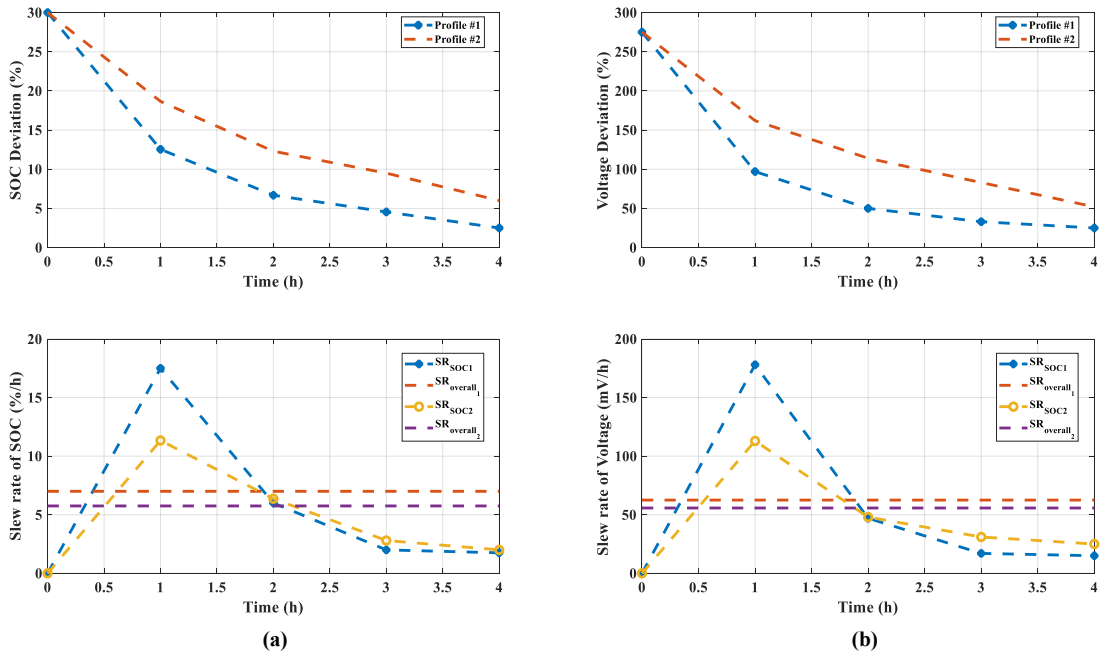


Fig. 1.18 Slew rate of SOC and Voltage equalization: (a) SOC profiles of two equalizers with their slew rate profile; (b) Voltage profiles of two equalizers with their slew rate profile.

levels after the equalization process. The higher the DoVE or the DoSE is, the greater the equalization capability it will have. For example, if the cells are equalized within $20mV$ voltage deviation and 2% SOC deviation after the initial difference of voltage and SOC are $250mV$ and 30%, respectively, the calculated DoSE and DoVE are 93% and 92%, respectively.

- **Equalization speed**: To assess the equalization speed of the equalizer, the slew rate of SOC equalization (SR_V: mV/h) and the slew rate of the SOC equalization (SR_{SOC}: %/h) can be introduced. The slew rates are defined as

$$SR_V = \frac{\Delta V_{init} - \Delta V_t}{t_{process}} \tag{1.8}$$

and

$$SR_{SOC} = \frac{\Delta SOC_{init} - \Delta SOC_t}{t_{process}}, \tag{1.9}$$

where ΔV_{init} and ΔSOC_{init} are the initial voltage deviation and initial SOC deviation between the cells before the equalization; ΔV_t and the ΔSOC_t are the voltage deviation and SOC deviation between the cells at t-th time point after a certain measurement time, $t_{process}$. Because the equalization speed of the equalizers can be varied at every instant, SR_{SOC} and SR_V should be assessed periodically according to the SOC and Voltage deviation profiles during the equalization process. For illustrative purposes, the operation profiles of two equalizers and their calculated slew rate indices are illustrated in Fig. 1.18. Vividly, the overall slew rate of both equalizers is almost similar but the slew rate after 1h shows the superiority of the equalizer #1. In this case, equalizer #1 did most of the work just during the first 1h, while the equalizer #2 needs more time to do the same task. Hence, equalizer #1 is better than equalizer #2 in terms of the equalization speed.

•**Coulombic Efficiency**: Because the operations of the equalizers in the actual applications are different from each other, it is difficult to assess the effectiveness of the individual equalizer. In addition, the operating waveform of the different equalizers is also heterogeneous, and thus, there is no common calculation of the efficiency of the equalizer. In order to assess the effectiveness of the entire equalization system, the Coulombic efficiency is adopted, which is calculated based on the total changed charge of the cells after the equalizing process. The operating principle of the SET-E has the same concept as shown in Fig. 1.19(a), where B_1 transferred a $Q_{discharge}$ to the energy tank. In addition, energy tank transferred a Q_{charge} to B_2 in the opposite way, which reflects the equalizing process. Based on the SOC profiles of the cells, the total changed charges of every cell, as shown in Fig. 1.19(b), are calculated by

$$d_{bk} = (SOC_{bk\_init} - SOC_{bk\_final})Q_{bk}, \tag{1.10}$$

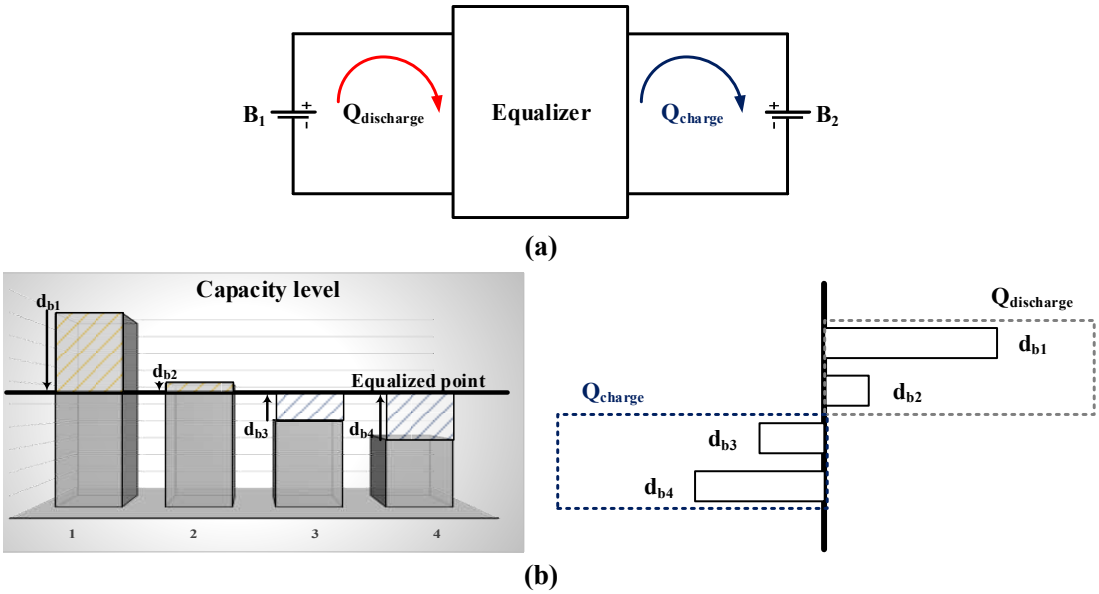


Fig. 1.19 Total changed charge concept: (a) charge transferring during the equalizing operation; (b) Total changed charge of the cells.

where SOC_{bk_init} is the initial SOC levels of the cell before the equalizing process, SOC_{bk_final} is the SOC level of the cell after the equalizing process, Q_{bk} is the actual capacity of the cell at the currently condition. Since there is a loss on the equalizer circuit during the equalizing process, Q_{charge} is less than $Q_{discharge}$, and thus, the Coulombic efficiency is expressed as

$$\eta_{Cou} = \frac{Q_{charge}}{Q_{discharge}}. \tag{1.11}$$

• **Performance stability**: Since the aging patterns of the cells are different and the energy distribution of the cells in the series string is arbitrary, the equalizer must be implemented in various test scenarios in term of energy distribution and numbers of cells. From many initial scenarios, three typical equalization scenarios are illustrated in Fig. 1.20(a), (b), and (c), respectively. In these cases, the initial energy of the cells has a descending, convex, or concave

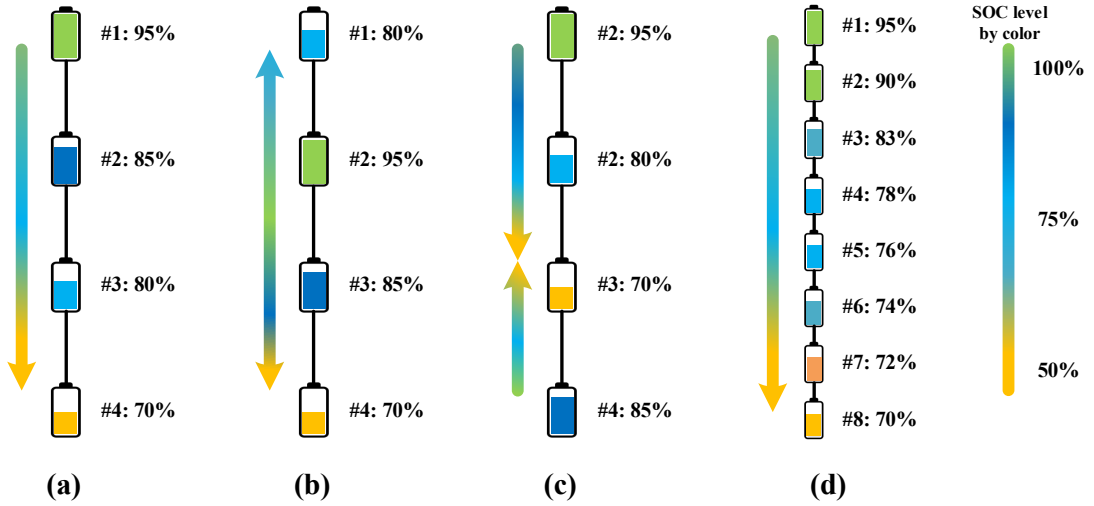


Fig. 1.20 SOC distribution of the cells in various scenarios: (a) Four cells in descending order; (b) Four cells in convex order; (c) Four cells in concave order; (d) Eight cells in descending order.

distributions. A good equalizer should have similar performance indices such as equalization capability, equalization speed, and energy loss for all scenarios. On the other hand, the number of cell also affect the performance of the equalizers. In Fig. 1.20(d), the energy distribution of eight series cells is shown. When comparing the performance consistency, an optimal topology can be selected. In Chapter 3, a case study is conducted to compare the performance of various topological configurations.

- **Component count, volume, and cost**: there is a correlation between the component counts, the volume, and the cost of the equalizer. Since the component counts of the equalizer are high, the equalizer will have a large volume and high cost. It raises a requirement for the developer to improve the equalization performance with cost and volume reduction. On the other hand, a high-performance equalizer sometimes requires a high cost. Therefore, the cost barrier can affect the decision of chosen topology configuration.

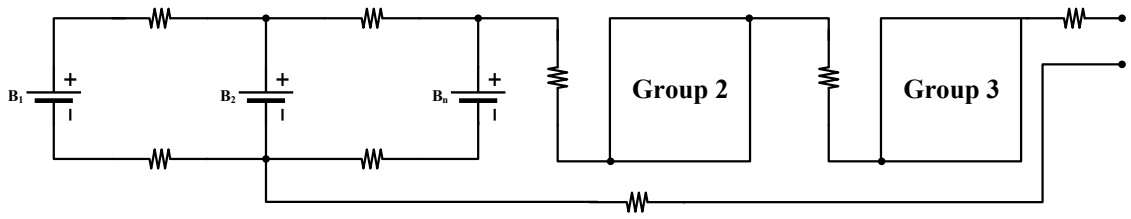


Fig. 1.21 Inconsistency between the cells and groups due to the packing process.

1.7 Level of Equalization for the Battery System

The cell-inconsistency has a high impact on the performance of the battery system when the number of cells is large. The inconsistency between the cells are the results of various factors, including the initial energy level and the maximum capacity of the cell after the manufacturing process, the packing process, and aging process.

• Due to the manufacturing tolerance of the cells, the impedance and the capacity of the cells are dissimilar. In general, the difference in open circuit voltages between the cells is approximately $50mV$ [74], and more in the dynamic condition.

• Although the manufacturing tolerance can be mitigated by the characteristic screening process, the inconsistency is indirectly increased during the packaging process. As the cells are connected in series and in parallel, the internal resistance of the connector and wiring may cause another inconsistency between the connections. This mechanism is illustrated in Fig. 1.21, where the resistance of the interconnecting wire can cause the mismatch in the parallel-connected cells as well as in the series connected groups. Thus, the cell-inconsistency can be more serious under dynamic operation conditions, although the cell open circuit voltages are almost similar.

• If the operating conditions such as current and temperature of the cells are dissimilar, their aging patterns also become mismatched and make the cell-inconsistency more serious.

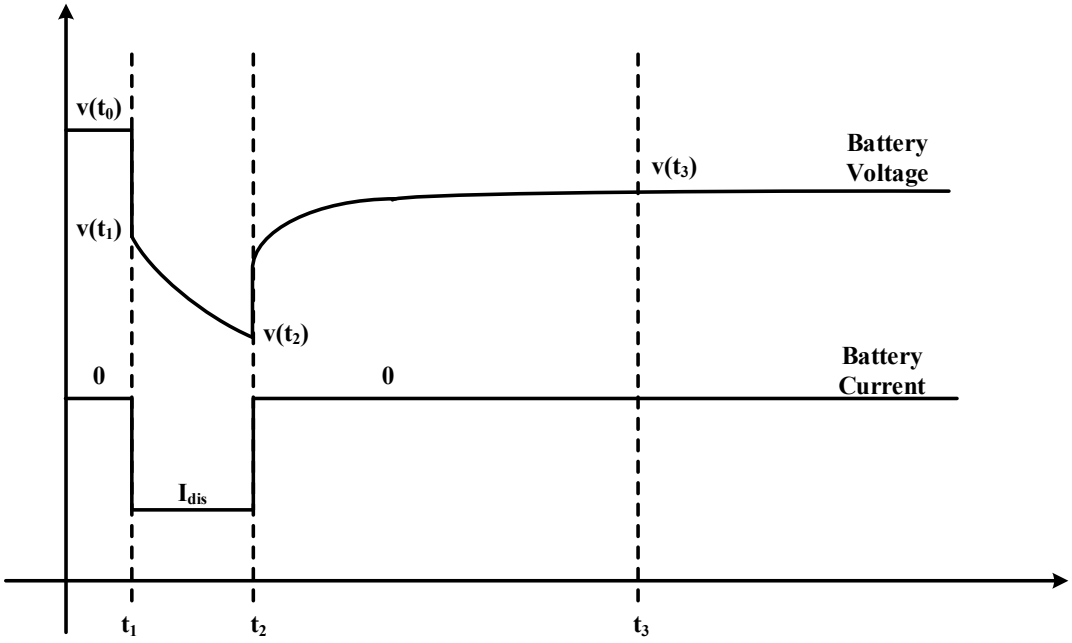


Fig. 1.22 Polarization effect of the battery during the discharging operation.

That's why the cell-inconsistency of the cells in the retired EV is observed, although the equalizer exists [3]. Thus, a high-performance and efficient battery equalizer is required to prolong the lifetime of the battery system.

On the other hand, the polarization effect of the cell voltage exists during the operation or balancing process. For illustrative purposes, the discharging process of a cell is shown in Fig. 1.22. Immediately after the discharge current is applied to the cell, its voltage drops as a result of the internal polarization impedance. When the discharge current is maintained, the polarization capacitance is charged, and thus, the cell voltage is continuously reduced. When the discharge current is removed, the cell voltage is gradually recovered until the polarization capacitance is fully discharged. Since the polarization impedance of the cell is large, the cell requires a lot of time to recover its steady state condition. Thus, the voltage comparison-based balancing techniques sometimes cannot guarantee a complete equalization

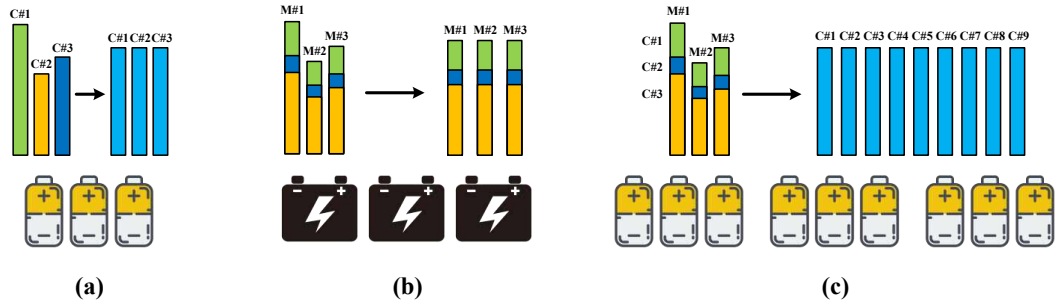
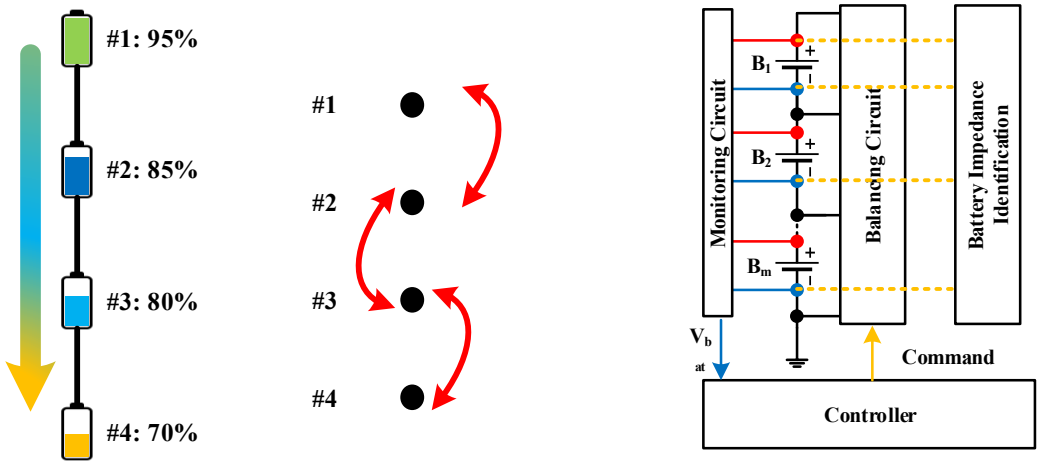


Fig. 1.23 Inconsistency and equalization level classification: (a) Level I: Cell-to-cell equalization; (b) Level II: Module-to-module equalization; (c) Level III: all cells in every module equalization.

between the cells. It means that the inconsistency between the cells always exists and will become higher at the module-to-module level.

Since the battery system is divided into various modules for better equalization and management, the level of equalization also needs to be defined. In this thesis, the equalization is divided into three levels as in Fig. 1.23. Equalization level I refers to the state where the energy levels of every cell inside a module are equalized within a predefined level (Fig. 1.23(a)). Next, the energy levels of the modules are equalized but the cell equalization is not considered at level II as in Fig. 1.23(b). Finally, level III refers to the condition in which the energy level of every cell in every module is equalized within a predefined deviation as in Fig. 1.23(c). If the BMS is able to achieve the level I and level II simultaneously, level III can be satisfied. In this thesis, various equalization strategies are proposed to achieve equalization level I and level II for the battery system with multiple modules in the series as well as the parallel.



(a) (b)

Fig. 1.24 Remaining problem of conventional structure of BMS: (a) impact of energy distribution to the equalization; (b) complete block diagram of a BMS

1.8 Problem Identification

1) Obviously, as the generative energy schemes, the switched-energy-tank equalizers (SET-Es) have more advantages than the dissipative energy schemes in terms of energy savings. However, the performance stability of the equalizer under various numbers of cells or initial energy contribution has not yet been fully considered. For example, the energy level of the cells is distributed in a descending order as in Fig. 1.24(a), where the highest-voltage cell and the lowest-voltage cell are at the opposite ends of the series string. Since most SET-E only focus on balancing the energy of two adjacent cells, energy must be transferred through many intermediate steps. Therefore, the loss of energy during the equalization and the executing time are significant. That's why it is essential to have an advanced equalizer that can directly transfer energy from the high-voltage cell to the low-voltage cell.

2) On the other hand, the modular structure of the battery system still has a potential risk for inconsistency between the modules, although the cells inside each module are completely equalized. Thus, an advanced equalizer topology for both cell and module levels is essential.

3) Unified evaluation indices, including performance stability, are essential for comparing the performance of various equalizers. It can accelerate the development process when various designs and configurations of the equalizers can be tested and compared at a fast speed.

4) The modular equalization strategies for both series and parallel connected battery modules are required to ensure the safety.

5) To monitor the cell aging, a complex management circuit is required, as shown in Fig. 1.24(b), which increases the total cost of the BMS.

1.9 Objectives and Contributions of the Thesis

This thesis aims to develop the switch-matrix active equalization for modular battery energy storage systems and to mitigate the cell-inconsistency with high performance in terms of equalization capability, speed, performance stability, and efficiency.

Based on the research motivation, the thesis has presented the theoretical operating principle and design consideration of the modular equalizer. The contribution of the thesis is as follows:

- The SMC-E is introduced in terms of theoretical operation principle, equalization strategy and control algorithm, and design considerations.
- A fast evaluation method is developed to compare the performance of various types of equalizers in long-term operations.

• The design of the SMC-E is modified for the series-connected module equalization. An autonomous equalization strategy is proposed to balance the energy of all cells in the pack. As well, the design considerations for the module levels are provided.

• The same SMC-E design can be re-utilized for the parallel-connected battery modules. The proposed topology can mitigate the impact of the inconsistency between the branches. Besides, the inrush current during the hot-swap process is also addressed.

• The proposed modular structures of the equalizer are implemented to verify the performance by both simulation and experimental results.

1.10 Outlines of the Thesis

Chapter 1 introduces the configuration of the battery cell in the pack and the impact of the cell-inconsistency on the battery system performance. In addition, the balancing techniques are classified according to their operation scheme while the monitoring and protection circuit of the individual cell is described. Hence, the technical limitation and disadvantages of the conventional BMS are determined in the requirement for the BMS considering the aging and cell-inconsistency. The performance assessment criteria are also introduced to systematize the development of the equalizer.

Chapter 2 describes the topological configuration and the control algorithm of the SMC-E unit to mitigate the cell-level inconsistency. In addition, a design guide is provided to ensure the performance of the SMC-E.

Chapter 3 introduces two effective verification methods for the performance assessment of equalizers. While the RTSS can emulate the equalization with high accuracy, the UA-model-based simulation can assess the long-term equalization in a short time.

Chapter 4 is the extension of the SMC-E unit for the series and parallel connected modules to achieve equalization level II and level III. The topological configuration and balancing strategies of the modular equalizer network are introduced.

Chapter 5 concludes this thesis and suggests several topics related to the BMS.

Chapter 2

Switch-Matrix Capacitor Equalizer for Cell Equalization

To mitigate the inconsistency at the cell level, the switch-matrix active equalization strategies are proposed. In this chapter, an advanced topological configuration for the cell equalization is chosen based on the requirement from Section 1.8. Next, the design consideration of the switch-matrix capacitor equalizer (SMC-E) is presented and verified in Section 2.1. The operating principle and control algorithm of the SMC-E is described in Section 2.1.1 and 2.1.2, respectively. In addition, the design consideration for the SMC-E is discussed in Section 2.2 and is verified in Section 2.3.

2.1 Proposed Switch-Matrix Capacitor Equalizer

To mitigate the inconsistency in cell level, the switch-matrix capacitor equalizer (SMC-E) is proposed. Since the battery system is divided into multiple sub-modules, an SMC-E is adopted to equalize the energy level of the cells inside a module. In addition, the switch-matrix

of the SMC-E is re-utilized to exchange the energy of the sub-module with other modules. In this Section, the operating principle and design of the SMC-E are provided.

2.1.1 Topological Configuration and Equalization Principle

The proposed SMC-E consists of one switch-matrix to determine the route of energy flow, a capacitor serving as the energy tank, and a sensing circuit to decide the switching pattern as in Fig. 2.1. Before every equalization, a scanning step is executed to predict the location of the highest-voltage cell and the lowest-voltage cell. Based on the scanned data, the optimal pairing algorithm inside the BMS will decide on the optimal switching pattern to achieve the highest equalizing speed.

By virtue of the switch-matrix, energy can be directly exchanged between any two cells in the series string. The operating principle concept in Fig. 2.1(b) describes the energy exchange of cell #1 and #3. The equalization capacitor is charged by the higher voltage cell in Phase A. When the switching pattern is changed in Phase B, energy is transferred from the capacitor to the lower voltage cell. The process is repeated in multiple cycles, and thus, the energy levels of the two cells are equalized. The same procedure is applied to the other cells to achieve the equalization condition for all cells.

Since the switch-matrix structure can deliver the energy from any-cell to any-cell directly, both autonomous control and governed control methods can be adopted. However, in view of the equalization strategy, the fastest strategy is to directly transfer energy from the highest voltage cell to the lowest voltage cell. Therefore, a governed control method is chosen to achieve the highest equalization speed and equalization capability.

The operation of the SMC-E is analyzed based on the equivalent circuit in Fig. 2.2. For an instant, R_1 and R_2 are the loop resistance including the wiring resistance, battery

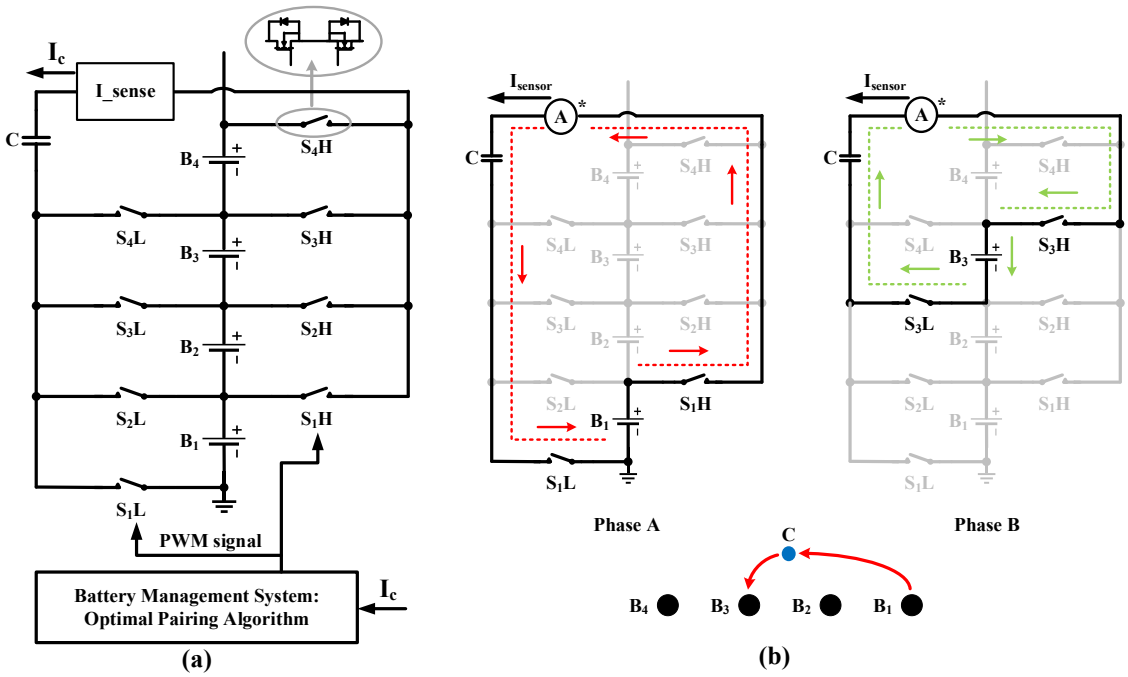


Fig. 2.1 Proposed Switch-Matrix Capacitor Equalizer: (a) Topology configuration ; (b) Operation principle of one equalization cycle.

impedance, the ESR of the energy tank, and the on-resistance of the MOSFET. Denote that τ_k (k=1, 2) is the time constant of the $R-C$ circuit and $v_c(t)$ is the instantaneous voltage of the capacitor. Thus, the instantaneous current in the cell #1 is expressed as

$$\tau_1 = R_1 C, \tag{2.1}$$

$$i_1(t) = \frac{V_{B1} - v_c(t_0)}{R_1} exp(\frac{-t}{\tau_1}). \tag{2.2}$$

Next, the amount of charge stored in the capacitor from the cell #1 is calculated by

$$\begin{aligned} Q_{in} &= \int_{t_0}^{t_1} i_1(t)dt \\ &= C\left(V_1 - v_c(t_0)\right)\left(1 - exp(\frac{-D_1}{f_{sw}\tau_1})\right), \end{aligned} \tag{2.3}$$

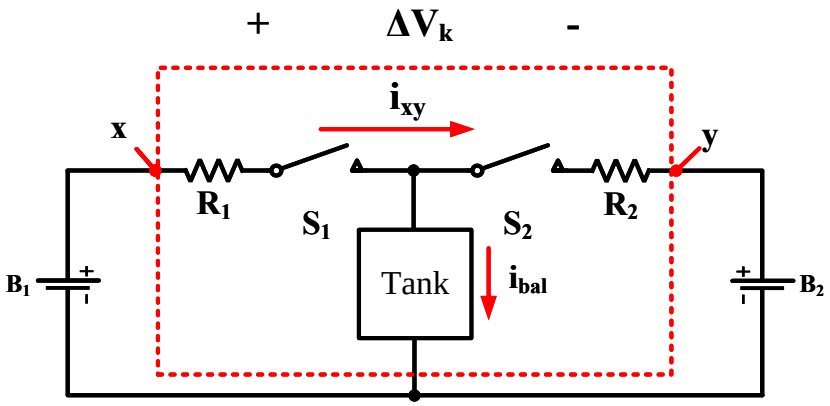


Fig. 2.2 Equivalent circuit of the SMC-E during the equalization

where f_{sw} is the switching frequency of the switches, and D_1 is the duty cycle ratio of the control signals in the phase A.

Similarly, the instantaneous current and the charge income of cell #2 are respectively calculated by

$$\tau_2 = R_2 C, \tag{2.4}$$

$$i_2(t) = \frac{v_c(t_2) - V_{B2}}{R_2} exp(\frac{-t}{\tau_2}), \tag{2.5}$$

$$\begin{aligned} Q_{out} &= \int_{t_2}^{t_3} i_2(t)dt \\ &= C(v_c(t_2) - V_{B2}) \left(1 - exp(\frac{-D_2}{f_{sw}\tau_2})\right) exp(\frac{-1}{2f_{sw}\tau_2}). \end{aligned} \tag{2.6}$$

On the other hand, the time constant τ_1 and τ_2 are much larger than the period of one equalization cycle. Hence, the theoretical waveform in Fig. 2.3 shows that the average capacitor voltage is approximately equal to the average of two cell voltages.

$$V_{c\_avg} = \frac{D_1 V_{B1} + D_2 V_{B2}}{D_1 + D_2}. \tag{2.7}$$

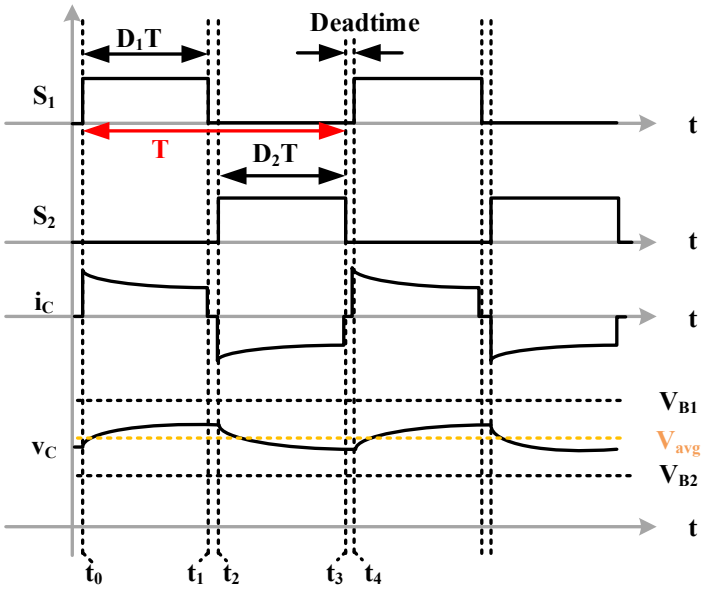


Fig. 2.3 Theoretical waveform of the SMC-E.

Assuming that $D_1 = D_2$, the average balancing currents of the cells #1 and #2 are calculated by

$$\begin{aligned} I_{avg1} &= Q_{in} f_{sw} \\ &= C f_{sw} \left(V_{B1} - V_{c\_avg}\right) \left(1 - exp(\frac{-D_1}{f_{sw}\tau_1})\right) \\ &= \frac{1}{2} C f_{sw} \left(V_{B1} - V_{B2}\right) \left(1 - exp(\frac{-D_1}{f_{sw} R_1 C})\right), \end{aligned} \tag{2.8}$$

$$\begin{aligned} I_{avg2} &= -Q_{out} f_{sw} \\ &= -C f_{sw} \left(V_{c\_avg} - V_{B2}\right) \left(1 - exp(\frac{-2D_2}{f_s \tau_2})\right) exp(\frac{-1}{2 f_{sw} \tau_2}) \\ &= \frac{1}{2} C f_{sw} \left(V_{B2} - V_{B1}\right) \left(1 - exp(\frac{-D_2}{f_{sw} R_2 C})\right) exp(\frac{-1}{2 f_{sw} R_2 C}). \end{aligned} \tag{2.9}$$

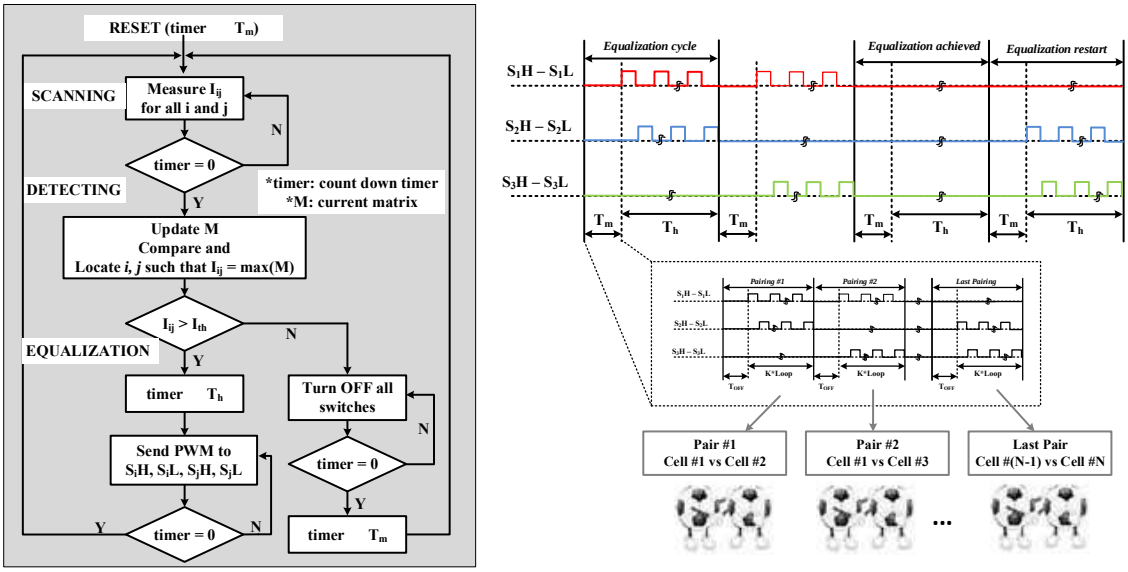


Fig. 2.4 Optimal pairing algorithm: (a) Control flowchart; (b) Timing diagram of the current scanning process.

Table 2.1
BALANCING-CURRENT MATRIX

	B_1	B_2	B_3	...	B_N
B_1	X	$\|I_{12}\|$	$\|I_{13}\|$	...	$\|I_{1N}\|$
B_2	$\|I_{12}\|$	X	$\|I_{23}\|$	...	$\|I_{2N}\|$
B_3	$\|I_{13}\|$	$\|I_{23}\|$	X	...	$\|I_{3N}\|$
...	...	...	...	X	...
B_N	$\|I_{1N}\|$	$\|I_{2N}\|$	$\|I_{3N}\|$	...	X

***X: not available.**

2.1.2 Optimal Pairing Algorithm for Equalization Strategy

In general, the voltage of the cells is monitored by the BMIC circuits to decide the equalizing strategy [75–80]. Since the BMIC-based monitoring system is compact and can monitor multiple cells at the same time, the control algorithm for the SMC-E is simple. However, the polarization effect during the operation and the electromagnetic noise can affect the measurement value, and thus, can make the wrong decision for the equalization strategy. In

this Section, an optimal pairing algorithm is proposed, which only requires one current sensor and replaces the BMIC circuit.

The optimal pairing algorithm is divided into multiple equalization cycles. In every cycle, three main processes such as scanning-detecting, and equalization, are executed as in Fig. 2.4(a). Based on the equations (2.8) and (2.9), the amplitude of the balancing currents depends on the voltage deviation between two cells. The higher balancing current, the higher voltage deviation will be. In other words, the switching pattern of the highest voltage cell and lowest voltage cell is determined through the scanning and detecting processes. For an instant, the timing blueprint of the current scanning process is illustrated in Fig. 2.4(b). Similar to a football league, the cell #1 and cell #2 form a pair, which is controlled by the switching pattern #1. The switching pattern is held in a K-loop to get a steady state balancing current, I_{12}, and the measured current is stored into a balancing current matrix as in Table 2.1. Next, all switches are turned off to let the cells recover their steady state condition during, T_{off}. Next, cell #1 continuously keeps the home-cell role and is paired with the new away-cell, cell #3. By the same token as the first pair, the balancing current of cell #1 and cell #3, I_{13}, is obtained and stored. When the cell #1 is already paired with all other cells, the cell #2 takes the role of home-cell and is paired with the other cells to scan the possible balancing current. Finally, a full balancing current matrix is formed as in Table 2.1 after the last pair is scanned.

After the balancing current matrix is formed, a comparison algorithm is executed to determine the optimal pair which results the highest balancing current, I_{opt}. The corresponding switching pattern of the optimal pair will be set for the switch-matrix and is held during T_h. After that, another scanning and detecting process is executed to redetermine

the optimal pair. Because the cell voltages change during the equalization process, the optimal pair will be dynamically modified. When the optimal balancing current, I_{opt}, is lower than a predefined threshold level, the energy levels of the cells are regarded as equalized and all switches are turned off. Due to the polarization effect, the battery voltage will be recovered after the equalization is stopped. To ensure the equalization condition, the scanning and detecting processes are periodically triggered to detect the cell-inconsistency level. The equalization process for the optimal pair will be executed again when I_{opt} becomes higher than the predefined threshold level. Because the scanning-detecting process can be periodically executed in the background, the other processes of BMS such as monitoring and protection are not disturbed.

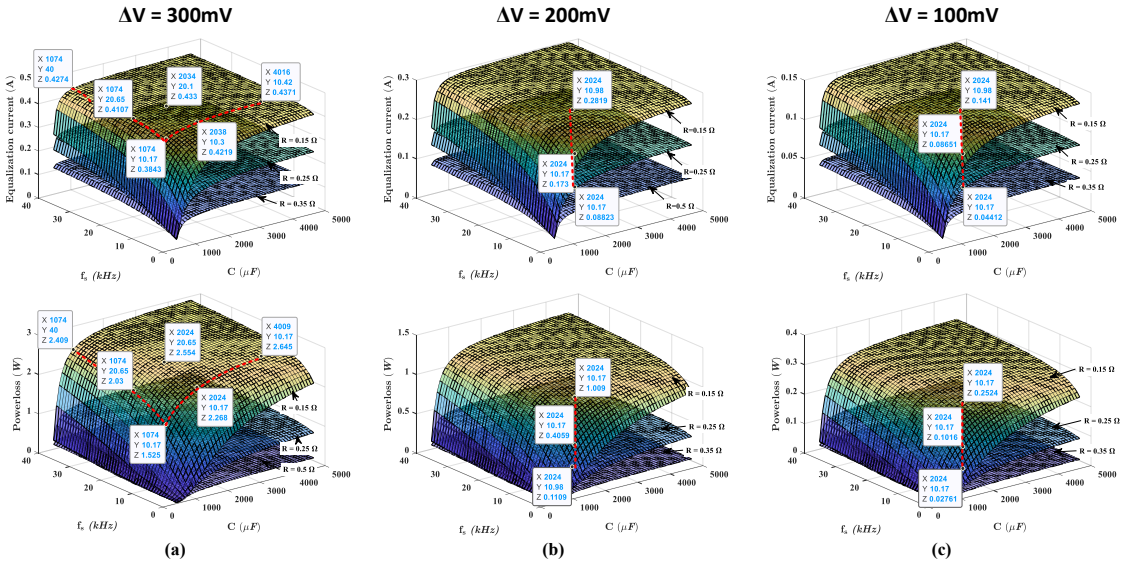


Fig. 2.5 Average balancing current and power loss of the SMC-E for two cells: (a) $\Delta V = 300\text{mV}$; (b) $\Delta V = 200\text{mV}$; (c) $\Delta V = 100\text{mV}$.

Table 2.2 DESIGN PARAMETER SUMMARY

	C	f_{sw}	$R_1 = R_2$	ΔV
$Parameter$	$470\mu F \sim 4700\mu F$	$500Hz \sim 40kHz$	$0.15\Omega; 0.25\Omega;$ *and* 0.5Ω	$300mV; 200mV;$ *and* $100mV$

2.2 Optimal Design Consideration for the SMC-E

To achieve high performance for the SMC-E, the circuit and operating parameters of the equalizer must be analyzed in terms of component size and cost.

2.2.1 Switching Frequency and Equalization Capacitance

In the SMC-E, the switching frequency of the switches, the capacitance of the balancing capacitor, and the internal resistance of the circuit have a high impact on the average balancing current and energy loss. Thus, the average balancing current and loss must be assessed first. While the average current is calculated by (2.8), the power loss is calculated through the following procedure.

• In the SMC-E, the balancing current waveform of the cells is almost pulsating. Under this assumption, the average and RMS balancing currents are expressed as

$$I_{avg} = I_0 D, \tag{2.10}$$

$$I_{RMS} = I_0 \sqrt{D}, \tag{2.11}$$

where $D_1 = D_2 = D$ is the duty ratio of the control signals, and I_o is the peak value of the pulse current. Hence, the ratio of the RMS current to the average current is calculated by

$$K_{ar} = \frac{I_{RMS}}{I_{avg}} = \frac{I_0\sqrt{D}}{I_0 D} = \frac{1}{\sqrt{D}}. \tag{2.12}$$

In addition, the switches require a deadtime period to prevent the short through, and thus, the duty ratio is usually set by 0.45. Hence, the loss can be calculated as the measured average current multiple by K_{ar} of 1.49. Therefore, the power loss of the equalizer during an equalization cycle is calculated by

$$P_{loss} = K_{ar}(V_{B1} I_{avg1} - V_{B2} I_{avg2}). \tag{2.13}$$

The calculation is applied for three voltage deviation points ($\Delta V = 300mV$, $\Delta V = 200mV$, and $\Delta V = 100mV$), which represent the equalization condition of the cells. In addition, the circuit and operating parameters are summarized in Table 2.2, where f_{sw} is the switching frequency; C is the balancing capacitance, and R_1-R_2 are the internal resistance of the equalizer. The results are illustrated in Fig. 2.5, which shows the impact of each design parameter on the performance of the SMC-E.

First of all, the amplitude of the average balancing current is strongly dependent on the voltage deviation between two cells. The balancing current is significantly reduced when the voltage deviation is lower than $100mV$, prolonging the equalization time. On the other hand, the average balancing current is increased when C and f_s have increased. However, the increasing trend of the average current is almost saturated when C and f_s across $2000\mu F$ and $10kHz$, respectively. For illustrative purposes, the red dash line in Fig. 2.5(a) is used to mark the rising curve of the average balancing current and its power loss. By considering three design points such as $\#1: 1000\mu F - 40kHz$, $\#2: 2000\mu F - 10kHz$, and $\#3: 4000\mu F - 10kHz$ for $R = 0.15\Omega$ cases, the difference between the average currents are trivial. The same token is found in the order cases of voltage deviation as in Fig. 2.5(b) and Fig. 2.5(c). On the other hand, a large balancing capacitance, C, requires a high investment and circuit volume. It means that increasing C and f_s to a high rate is an ineffective strategy to enlarge the balancing current but only increases the cost and volume.

Secondly, the power loss of the equalization is assessed along with the average balancing current. In fact, the energy loss during the equalization must be assessed but it can only be calculated based on the operating profiles. Thus, the power loss is used to compare the loss of various design options. According to Fig. 2.5, although the balancing current is almost saturated, the power loss is significantly enlarged when f_s across $10kHz$ and C is higher than $2000\mu F$. Since the average balancing current and power loss are directly proportional, there is a trade-off between the equalization speed and the energy loss during the equalization. The higher the equalization speed, the more energy loss will be, and vice versa. By considering both average balancing current and power loss, four design combinations of

C and f_s are compared including design $\#1-1000\mu F/10kHz$, design $\#2-2000\mu F/10kHz$, design $\#3-2000\mu F/20kHz$, and design $\#4-4000\mu F/20kHz$.

Furthermore, Fig. 2.5 also shows a dependence of the average current on the internal resistance of the circuit. With the same design of C and f_s, the average current is dropped over 60% when R is changed from 0.15Ω to 0.5Ω in all cases of voltage deviation. Since the ESR of the capacitor takes up most of the internal resistance, the capacitor unit must be optimized in terms of configuration and volume. The equalizer can achieve a higher current just by reducing the internal resistance of the circuit, rather than increasing the equalizing capacitance or the switching frequency.

2.2.2 Balancing Capacitance and Capacitor Size

According to Fig. 2.5, the internal resistance of the circuit has a strong impact on the average balancing current. The internal resistance includes the on-resistance of the MOSFET, the resistance of the wiring and connector, and the effective ESR of the capacitor. Since the on-resistance of the MOSFET and the wiring resistance are almost fixed, the type of capacitor and the number of parallel connections must be carefully considered. However, the voltage rating of the capacitor is relatively low during the equalization application. Based on the comparison of the capacitor types in Fig. 2.6, the candidates can be aluminium electrolytic capacitors, tantalum capacitors, plastic film capacitors, and multi-layer ceramic capacitors.

Assuming the total capacitance and switching frequency are fixed as $2000\mu F$ and $10kHz$ from the simulation, the number of parallel capacitors is decided based on the capacitance of the single capacitor. For comparison, five design options of various capacitor types are assessed, including a $10\mu F$ tantalum capacitor, a $10\mu F$ MLCC , a $10\mu F$ film capacitor, a $10\mu F$ electrolytic capacitor, and a $100\mu F$ aluminum electrolytic capacitor. If the balancing

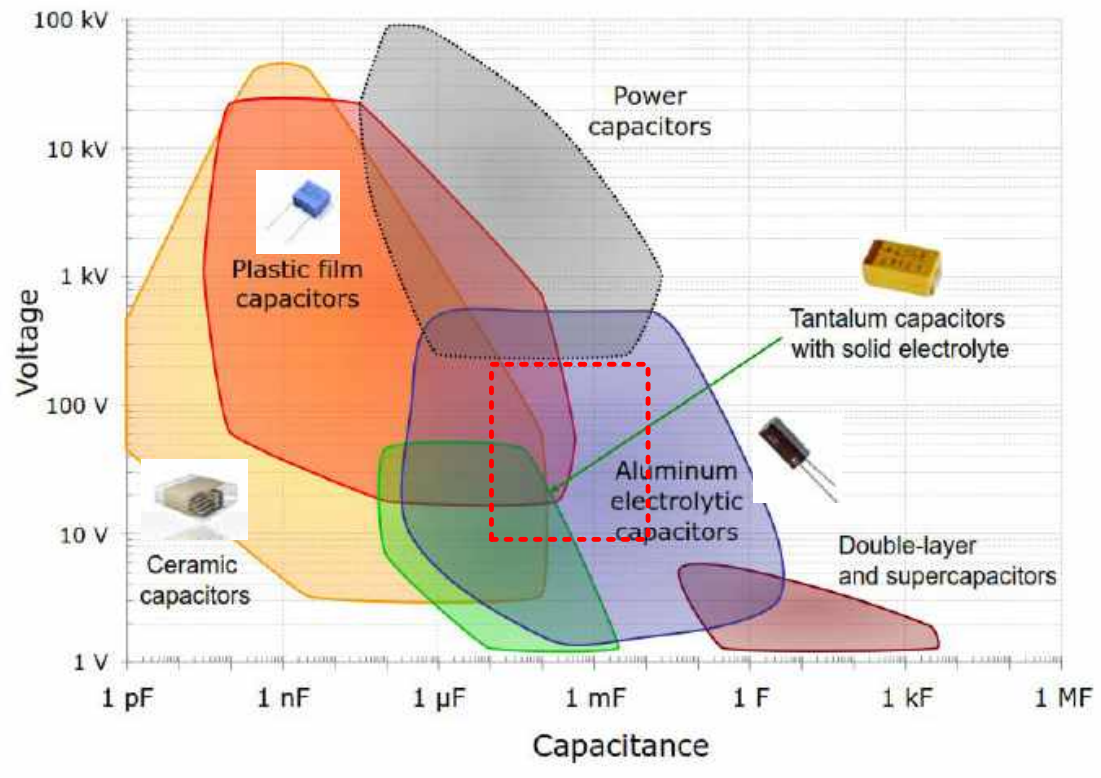


Fig. 2.6 Capacitor type comparison.

capacitor unit is utilized for modular equalization, a higher voltage rating of the capacitor is required. For example, a 50V rating capacitor is selected for a 4S1P battery string. However, it restricts the choice of tantalum and MLCC capacitors due to the limited energy density of the package from the manufacturer. The specifications for each option are summarized in Table 2.3 for comparative purposes. Based on the the loss tangent $tan\delta$ of the capacitor from their datasheet, the ESR of the capacitor is approximately calculated by

$$ESR = \frac{tan\delta}{\omega C}. \tag{2.14}$$

Table 2.3 CAPACITOR SIZING-OPTION COMPARISON

		Tantalum	**MLCC**	**Film**	**Elec.** #1	**Elec.** #2
Parameter of 1 cap.	C_{unit} $[\mu F]$	10	10	10	10	100
	V_{rating} $[V]$	50	50	50	50	50
	$tan\delta$	0.1	0.1	0.015	0.12	0.12
	$f[kHz]$	10	10	10	10	10
	$ESR_{unit}[m\Omega]$	159	159	23.8	191.1	19.1
	$Volume_{unit}[mm^3]$	118.1	14	1320	43.2	72.2
	Unit price $[KRW]$*	2,390	1,764	3,890	25	60
Parameter of N Cap.	N◇	200	200	200	200	20
	$ESR_{effective}$ $[m\Omega]$	0.8	0.8	0.12	0.96	0.96
	Total volume $[mm^3]$	23,625	2,800	264,000	8,635	1,444.5
	Total cost $[KRW]$	478,000	352,728	77,800	5,000	1,200

*Unit price is referred from Eleparts in October 2022.

◇ N is the number of parallel capacitors.

In addition, the number of parallel capacitor is calculated by

$$N = \frac{C_{target}}{C_{unit}}. \tag{2.15}$$

On the other hand, the impedance of the capacitor in parallel connection and its effective impedance are expressed as

$$Z_m = ESR_m - \frac{j}{2\pi f C_m}, \qquad m = 1,\ 2,...,\ N \tag{2.16}$$

$$Z_{effective} = \frac{1}{1/Z_1 + 1/Z_2 + ... + 1/Z_N}. \tag{2.17}$$

To simplify the calculation, the ESR and capacitance of the capacitors are assumed equal ($ESR_1 = ESR_2 = ... = ESR_N; C_1 = C_2 = ... = C_N$). Thus, the effective impedance and ESR

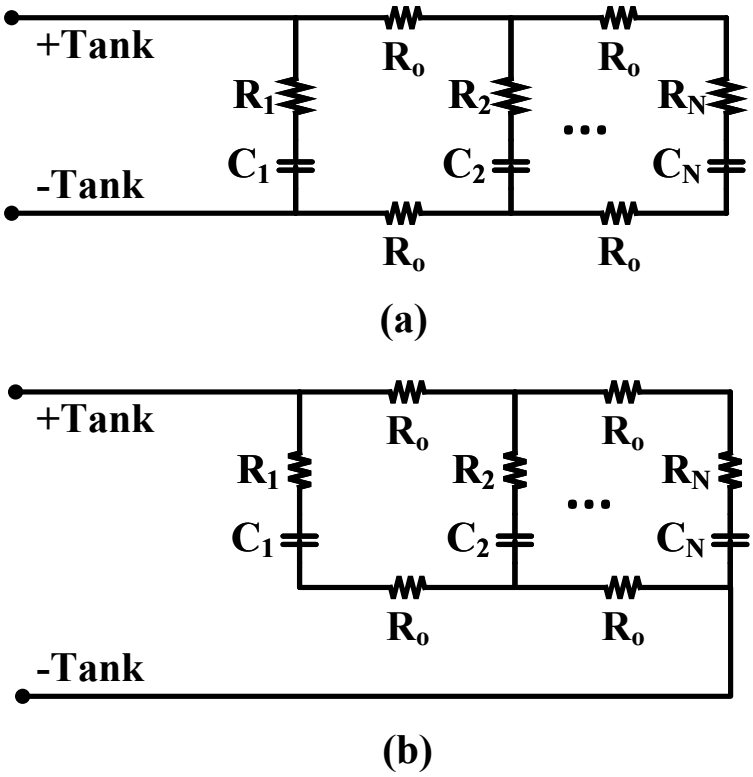


Fig. 2.7 Practical routing layout of parallel capacitors: (a) first-in/first-out; (b) first-in/last-out.

of the parallel capacitors are obtained as

$$Z = ESR - \frac{j}{2\pi fC}, \tag{2.18}$$

$$Z_{effective} = \frac{Z}{N} = \frac{ESR}{N} - \frac{j}{2N\pi fC}, \tag{2.19}$$

$$ESR_{effective} = real(Z_{effective}) = \frac{ESR}{N}. \tag{2.20}$$

On the other hand, the capacitor volume is calculated based on the standard dimension from their datasheet and is summarized in Table 2.3. The price of the capacitor is referred from the online website eleparts.co.kr in November 2022 based on 100 quantity MOQ. The

comparative table shows that the tantalum and film capacitors can achieve a low effective ESR but their volume and cost are too high to adopt. By comparing the MLCC with two options of electrolytic capacitors, the MLCC achieves a 20% of lower ESR but the cost is hundreds of times higher. Since the aluminium electrolytic capacitor has a long historical development, various capacitance and voltage rating parts can be found on the market at a low price. Therefore, 20 pcs. of $100\mu F$ aluminium electrolytic capacitors are connected in parallel for the design in this thesis.

During the hardware prototype making, the layout configuration of the capacitor is important. In general, the capacitors can be connected in parallel as first-in/first-out configuration as in Fig. 2.7(a). In this case, the stored energy of each capacitor is not homogeneous due to the parasitic resistance of the copper layer or the wiring. Thus, the temperature of the capacitor #1 is always higher than the others. To resolve this issue, the first-in/last-out configuration is recommended as shown in Fig. 2.7(b). In this configuration, the current flows evenly through every capacitor and the wire resistance.

Switch-matrix and Gating Control

To mitigate the impact of the energy distribution, the energy must be transferred between the highest voltage cell to the lowest voltage cell directly. Therefore, the switch-matrix structure is utilized. Two structures of switch-matrix can be utilized for the SMC-E, which are illustrated in Fig. 2.8. In the multiplexer structure in Fig. 2.8(a), two switches are utilized to connect a cell to the energy tank, C. For example, the switches S_1H and S_1L are turned on to connect cell #1 to the balancing capacitor, C, in a phase while the other switches are turned off. In the next phase, the switches S_1H and S_1L are turned off while the switches S_4H and S_4L are turned on to dock the cell #4 on the energy tank. In this case,

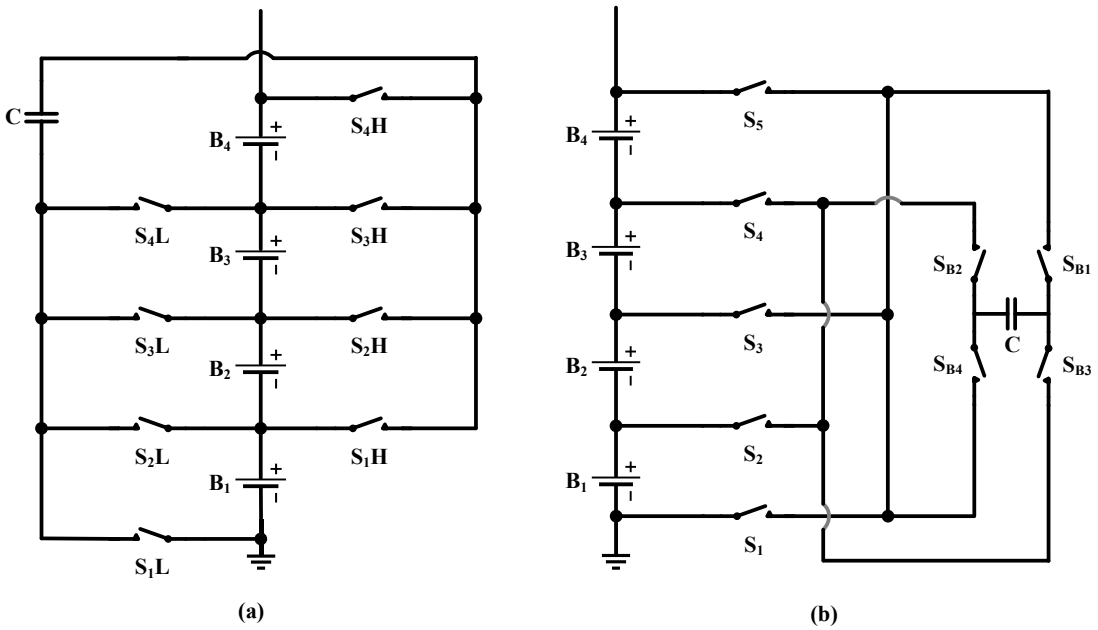


Fig. 2.8 Switch-matrix configuration: (a) Multiplexer structure; (b) Odd-Even structure.

there is an energy exchange between cell #1 and #4. In the multiplexer structure for N cells, $2N$ switches and N control signals are required to generate $\frac{N(N-1)}{2}$ combination patterns.

On the other hand, the odd-even structure in Fig. 2.8(b) turns on four switches in one phase to connect the cell to the energy tank. For example, the switches S_1, S_2, S_{B3}, and S_{B4} are turned on in phase A to connect cell #1 to the capacitor, C. In phase B, the switching pattern is changed as the switches S_4, S_5, S_{B1}, and S_{B2} are turned on while the others are de-activated to connect cell #4 to the energy tank. In view of the components count, the odd-even structure requires $N+5$ switches. Thus, it can reduce $N-5$ switches compared with the multiplexer structure when N is greater than 6. However, it requires $N+3$ individual control signals to control the equalizing operation, which increases the complexity of the control algorithm. In addition, the odd-even structure make the internal resistance of the circuit increase because there are four on-switch losses in one loop. By using equation (2.8)

Table 2.4 SWITCH-MATRIX STRUCTURE COMPARISON

Structure	Number of switches	Number of control signal	Number of activated switches
Multiplexer	2N	N	2
Odd-Even	N+5	N+3	4

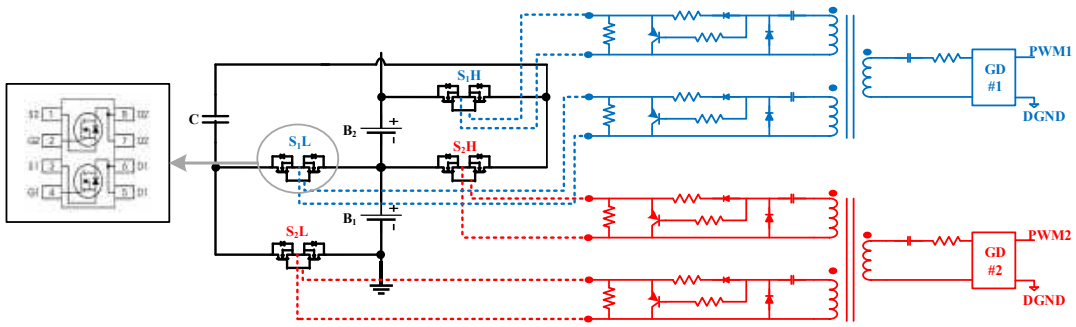


Fig. 2.9 Switch configuration and gating circuit

and (2.9) to calculate the balancing current, the odd-even structure has a lower current rating than the multiplexer structure.

For an instant, the comparison of the multiplexer and odd-even structures is summarized in Table 2.4. Since the control signal, including gate driver and PWM signals, takes more cost and volume, the multiplexer structure is chosen in this research for a simpler control circuit. In both structures of the switch-matrix, two MOSFETs are connected in back-to-back to ensure the bi-directional blocking, and thus, prevent the short circuit of the series cells. In addition, the floating ground for the gating circuit is required for every switch. Various gate driver techniques can be adopted, but the pulse transformer-based and floating DC-DC converter-based methods are two most popular techniques [81–83]. If the number of switches in the SMC-E is high, the pulse transformer-based gating method is more preferred because the floating DC-DC-based gate driver becomes expensive. The configuration of the switches and the gate driver is illustrated in Fig. 2.9.

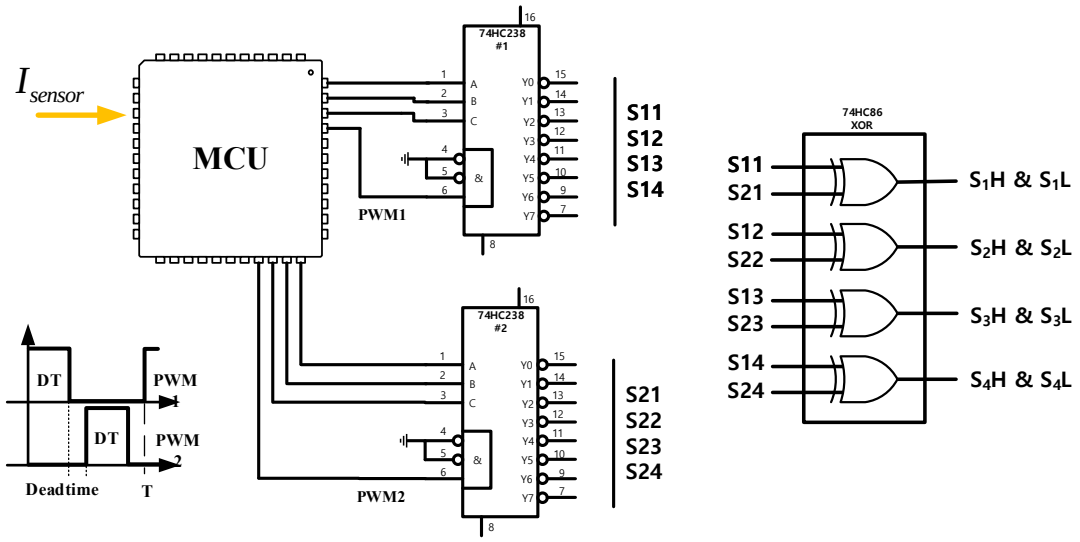


Fig. 2.10 PWM signal extension for SMC-E.

Table 2.5 TRUTH TABLE OF SIGNAL EXTENSION FOR 4S1P BATTERY STRING

IC_1-G1	IC_1-A0	IC_1-A1	IC_1-A2	IC_2-G1	IC_2-A0	IC_2-A1	IC_2-A2	PATTERN
$PWM1$	L	L	L	$PWM2$	H	L	L	#1 *vs.* #2
$PWM1$	L	L	L	$PWM2$	L	H	L	#1 *vs.* #3
$PWM1$	L	L	L	$PWM2$	H	H	L	#1 *vs.* #4
$PWM1$	H	L	L	$PWM2$	L	H	L	#2 *vs.* #3
$PWM1$	H	L	L	$PWM2$	H	H	L	#2 *vs.* #4
$PWM1$	L	H	L	$PWM2$	H	H	L	#3 *vs.* #4

Owing to the development of semiconductors, multiple MOSFETs can be integrated into one package which helps to significantly reduce the size of the switches. In this thesis, dual N-channel MOSFET NVMFD5485NL from Onsemi is used due to its low on-resistance and high current rating. On the other hand, the 1:1:1 pulse transformer controls two switches by a PWM signal. By virtue of the pulse transformer, the control signal is isolated from the power line.

Furthermore, the number of PWM control signals increases as the number of cell increases, but the common micro-controller unit (MCU) has a limited PWM signals. Since only two PWM signals are activated in an operation, a signal extension circuit is utilized and is

illustrated in Fig. 2.10. The signal extension consists of two demux IC groups to extend two PWM signals to multiple signals. For example, two demux IC can be used for 4 to 8 battery cells, where the complementary PWM signal pair from MCU is connected to the G1 pins of the demux ICs as their enable signal. Next, the output signals from demux ICs are merged by the XOR IC for each switch-pair in the switch matrix. As a result, only one cell can be connected to the energy tank in a phase of equalization. The truth table of the signal extension for a 4S1P battery string is summarized in Table 2.5. The more series connection there is, the greater required number of the demux IC will be. In this case, the demux and XOR ICs can be easily replaced with an FPGA chip, which significantly reduces the size of the extension circuit.

Current Sensing Circuit and Measuring Algorithm

Current sensing is an important part of the SMC-E when the measured current is utilized to predict the optimal pair. According to [84, 85], the most popular current measuring methods are known to use the shunt resistor and hall sensor as in Fig. 2.11(b) and Fig. 2.11(c). The shunt resistor-based method has a high accuracy due to its high bandwidth. However, the resistance of the shunt resistor can increase extra resistance to the circuit, and thus, reduce the balancing current. Furthermore, isolation is required for the pre-amplifier circuit since the ground reference of the current sensor changes according to the switching pattern. In contrast, the Hall sensor inherently isolates the ground of the sensing circuit from the power line of the SMC-E. In addition, the internal resistance increment when using a Hall sensor is also trivial. The critical issue of the hall sensor is its limited bandwidth, although some high-bandwidth integrated hall sensors can be found in industrial applications. However,

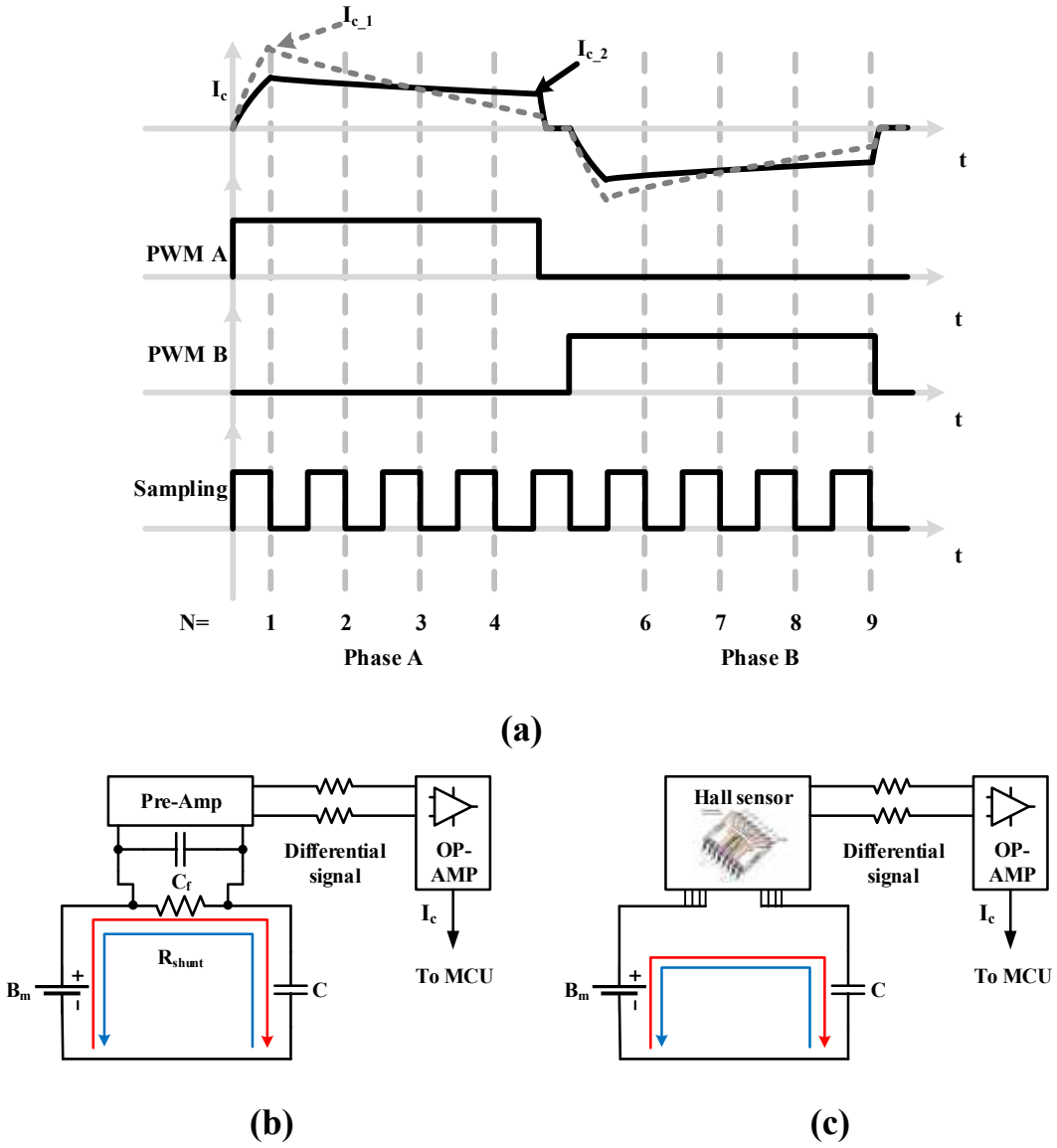
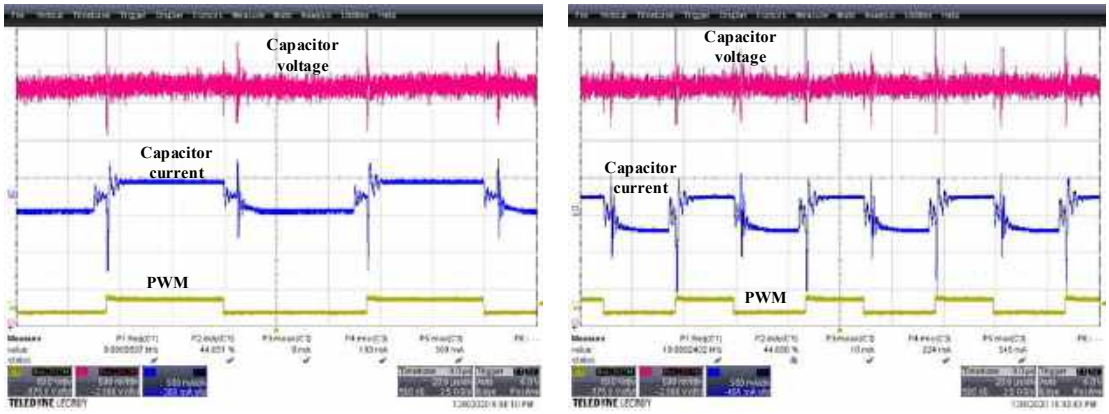


Fig. 2.11 Sampling diagram and current sensing circuit: (a) Sampling diagram; (b) shunt-resistor-based measuring method; (c) Hall-sensor-based measuring method.

since the optimal pairing algorithm requires only an average current instead of the high bandwidth waveform, Hall sensor can be a reasonable choice.

Due to the inconsistency between the cells, the shape of the current waveform of two different pairs can be heterogeneous as in Fig. 2.11(a). Thus, the sampling frequency of



(a) (b)

Fig. 2.12 Operation waveform of the SMC-E: (a) Design $\#1-1000\mu F/10kHz$; (b) Design $\#1-4000\mu F/20kHz$.

the current measurement must be at least 8 to 10 times faster than the switching frequency of the equalizer. In Fig. 2.11(a), the current is measured at four points in phase A, when $N = 1,\ 2,\ 3,\ 4$, and the average value of the measured current will be recorded to the memory. When the switching pattern is just changed, the measured currents from the first few equalization cycles should be ignored to let the balancing current reach the quasi-steady state. The cell-pair, which has the highest average current, will be assigned as the optimal pair and the corresponding switching pattern is decided.

2.3 Experimental Verification

To verify the performance of the SMC-E, a prototype for 4S1P battery string is built. Firstly, the optimal design will be assessed to verify the theoretical analysis. Next, the optimal pairing algorithm will be executed under various scenarios.

2.3.1 Design Verification

The equalization is executed for two cells, which have the voltage deviation is $320mV$ ($V_1 = 4.163$V; $V_2 = 3.843$V). Four design combinations are assessed including: design $\#1 - 1000\mu F/10kHz$, design $\#2 - 2000\mu F/10kHz$, design $\#3 - 2000\mu F/20kHz$, and design $\#4 - 4000\mu F/20kHz$. The internal resistance of the circuit including the battery internal resistance, the ESR of the capacitor, the on resistance of the MOSFET, and the resistance of the wiring are measured and calculated. The total resistance of the loop is 0.45Ω and the operation waveform of the design #1 and #4 is shown in Fig. 2.12. The balancing currents of the four cases are 193mA, 206mA, 212mA, and 224mA, respectively. In comparison with the balancing circuit in the theoretical analysis, the difference between the calculation and experiments is approximately 5%. Hence, the design equation in Section 2.2 is verified.

Based on the results, the impact of the switching frequency and the equalization capacitance on the balancing current is considered. Although the capacitance and switching frequency of design #4 are much higher than design #1, the difference in balancing current between the two designs is trivial due to the high internal resistance of the circuit. It means that the design of the capacitors and PCB layout to minimize the internal resistance of the circuit is more critical than increasing the balancing capacitance and switching frequency.

Furthermore, the SMC-E is implemented for 2 Li-po pouch cells (SK60 3.6V/60Ah). Compared to the cylindrical cells, the pouch cells have a much lower impedance ($1m\Omega$). The circuit parameters of the SMC-E are designed as $2,000\mu F/20kHz$. The capacitor current and voltage waveforms are shown in Fig. 2.13. In the experiments, the cell voltages in two cases are $3682mV - 3582mV$ and $3682mV - 3432mV$, respectively. Vividly, the operating waveforms of the SMC-E are similar to that of the cylindrical cells. With the same design,

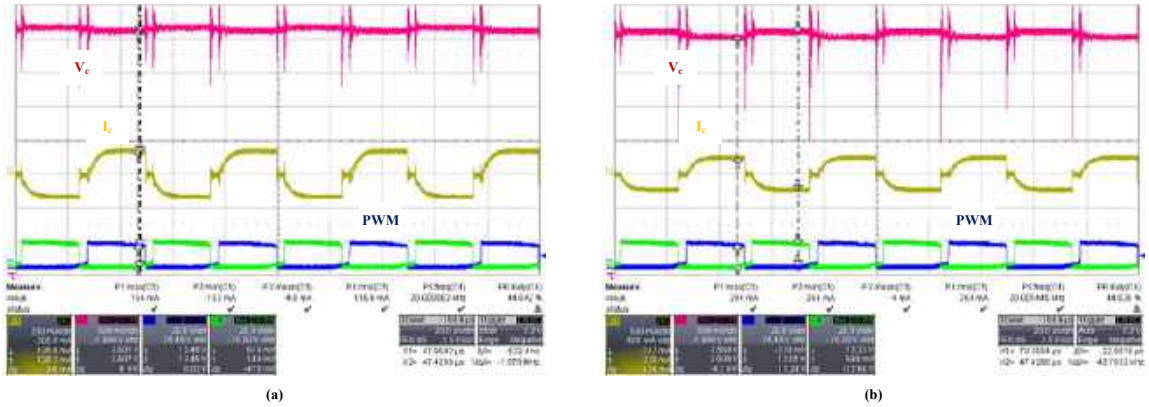


Fig. 2.13 Capacitor Current and Voltage waveform of SMC-E with Li-po pouch cell: (a) $\Delta V = 100mV$; (b) (a) $\Delta V = 250mV$.

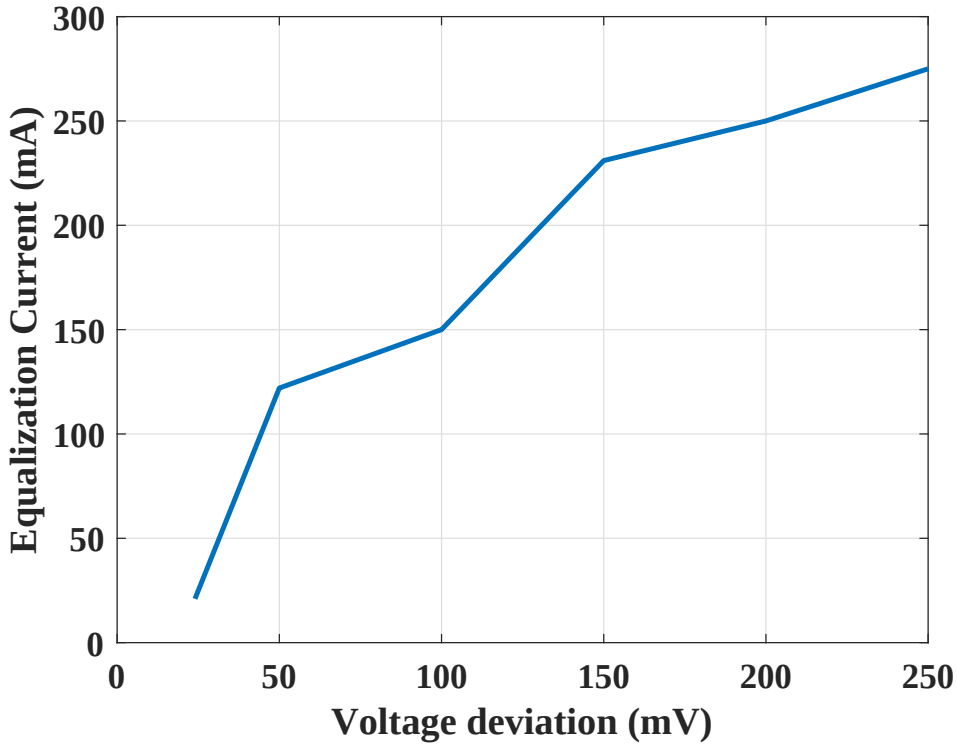


Fig. 2.14 Equalization current of SMC-E at various voltage deviation levels .

the equalizing currents of the SMC-E are measured at various levels of voltage deviation as in Fig. 2.14. Since the internal impedance of the pouch cells is lower than the cylindrical

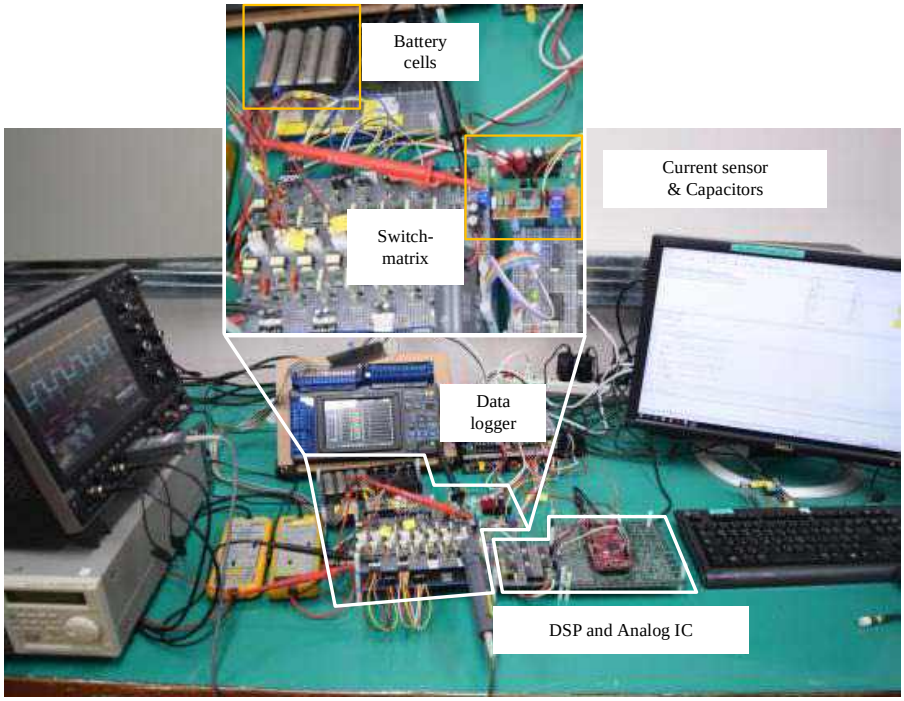


Fig. 2.15 Experimental Setup of SMC-E for four 18650 cells (3.6V-2.6Ah).

cells, the SMC-E can achieve a higher equalization current in the case of the pouch cells. Thus, the SMC-E can be applied to both cylindrical and pouch cells.

2.3.2 Performance Assessment

To verify the performance of the SMC-E, the optimal pairing algorithm is implemented in the hardware prototype. The switches are controlled by a DSP (TI-TMS320F28379D) and a signal extension circuit. The experiment setup is shown in Fig. 2.15, where the design $\#3-2000\mu F-10kHz$ is implemented and the cell voltages are recorded by a data logger (Hioki-LR8402-20) during the equalizing process. Next, the recorded data is plotted to assess the performance of the SMC-E. To observe the optimal pairing algorithm, the current and voltage of the capacitor is measured by the oscilloscope at $640ms/div$ time base while the detail waveform presents the actual value at $20\mu s/div$ time base. To emulate the

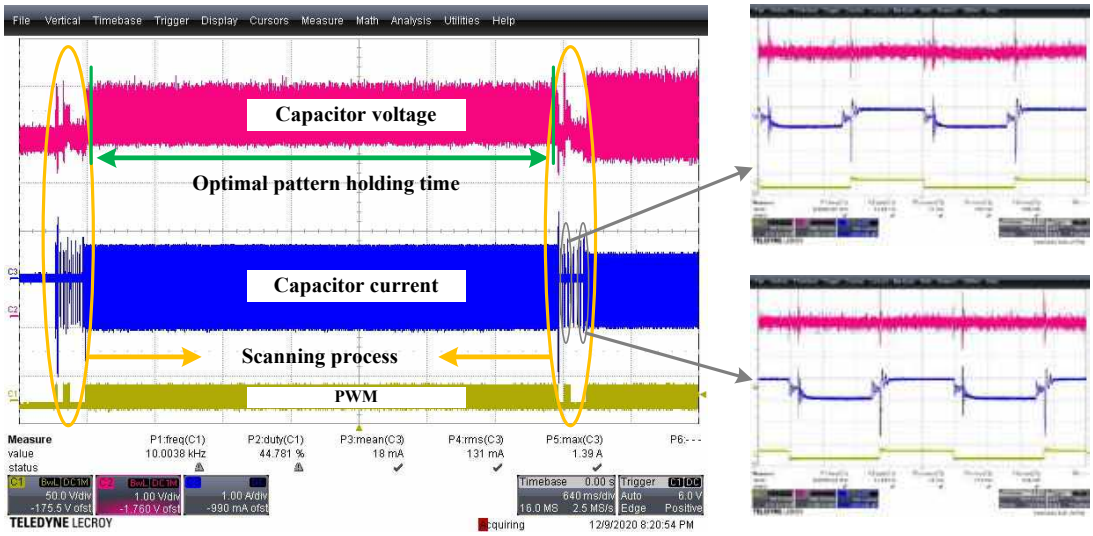
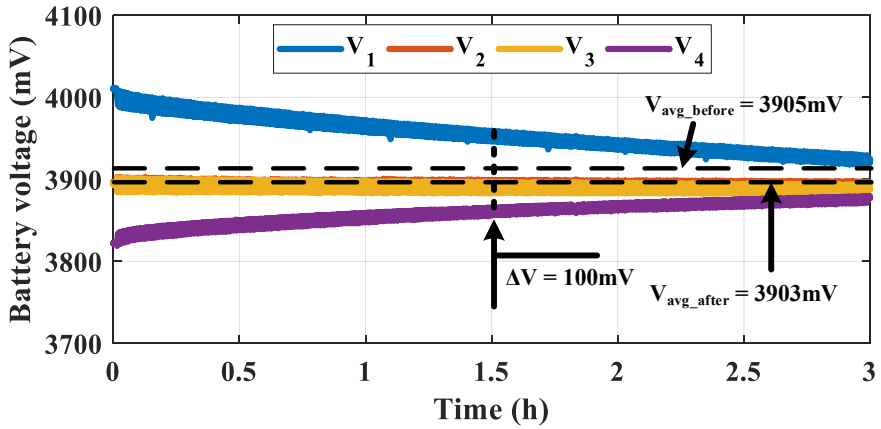


Fig. 2.16 Current and voltage waveform of the capacitor: (a) one equalization cycle-Timebase 640ms/div; (b) scanning waveform of two cell-pairings-Timebase 20μs.

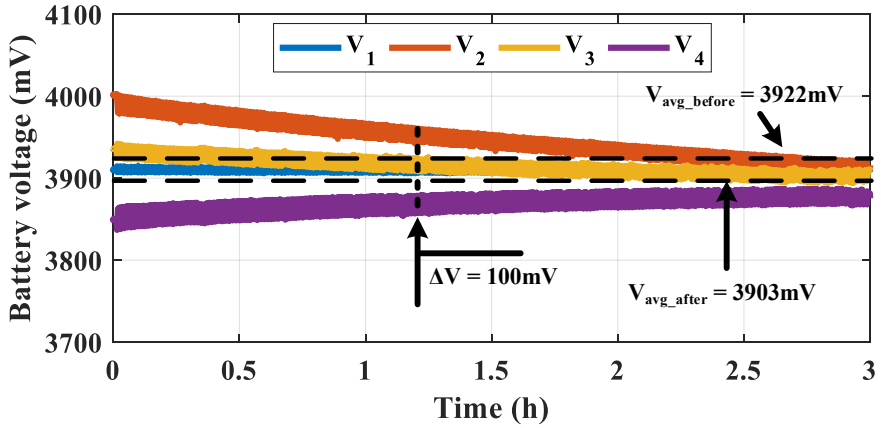
cell-inconsistency, the cells are fully charged, and then, are discharged at the predefined voltage levels. The initial voltage of the cells is summarized in Table 2.6.

The waveform in Fig. 2.16 represents the optimal pairing algorithm, where one equalization cycle is divided into two sub-processes. The balancing current of every cell-pair is scanned one-by-one to detect the optimal pattern. Therefore, the optimal pattern is maintained for a holding time for the energy exchange between the optimal cell-pair. Because the cell requires a long time to change its energy level, the holding time can be much longer than the scanning time without affecting the performance of the SMC-E. The total time for the scanning process is about 500ms, and thus, the holding time is set at 1 minute. Moreover, the long holding time can allow the other cells to recover the steady state voltage level, and thus, can increase the balancing current in the next cycle.

During the hardware experiments, only the voltage of battery cells can be recorded. Therefore, it is difficult to assess the DoSE and energy loss. Assuming that there is no loss



(a)



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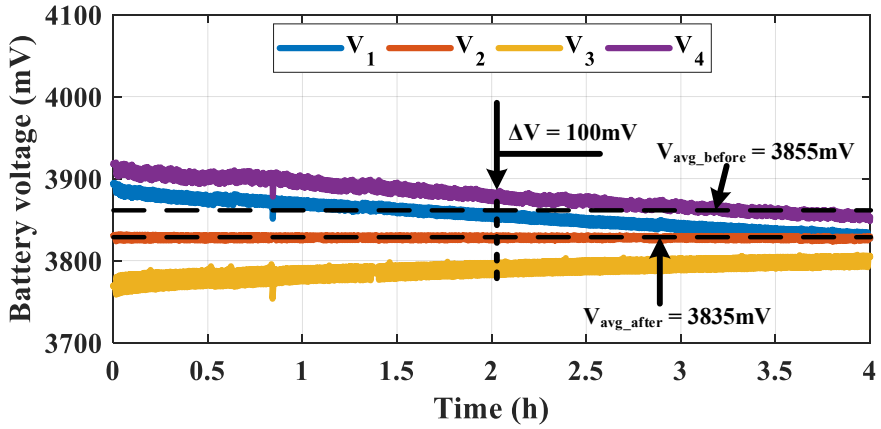


(c)

Fig. 2.17 Voltage profile of the cells in: (a) Case 1; (b) Case 2; (c) Case 3.

Table 2.6 EXPERIMENTAL RESULTS-BATTERY VOLTAGES (mV)

	Cell #1	Cell #2	Cell #3	Cell #4	V_{avg}	ΔV
Initial #1	4000	3900	3910	3820	3905	180
Exp. #1	3920	3900	3900	3895	3903.75	25
Initial #2	3900	4010	3940	3840	3922.5	170
Exp. #2	3910	3910	3905	3890	3903.75	20
Initial #3	3900	3830	3760	3930	3855	170
Exp. #3	3840	3840	3810	3850	3835	40

during the equalization, the cell voltages will be equalized to the average cell voltages at the initial condition. In the actual experiments, the average voltage after the equalization is lower than the initial average level due to the loss. Thus, the deviation of the average voltage of the cells before and after the equalization represents the loss. In this case, the voltage loss is calculated by

$$V_{avg\_before} = \frac{\sum_{k=1}^{N} V_{k\_before}}{N} \tag{2.21}$$

$$V_{avg\_after} = \frac{\sum_{k=1}^{N} V_{k\_after}}{N} \tag{2.22}$$

$$\Delta V_{avg} = V_{avg\_before} - V_{avg\_after}. \tag{2.23}$$

The results in Table 2.6 show that the voltage of the cells in three cases are equalized within $25mV$ after 3h of the equalization process in case #1 and case #2. On the other hand, the SMC-E requires more time to equalize the cell voltage within $40mV$ since the initial cell-inconsistency is difference to case #1 and case #2. The calculated DoVE index of the SMC-E after the equalization in all cases is 86%, 88.23%, and 76.47%, respectively. In addition, the voltage profiles of the cells in Fig. 2.17 show the relatively homogeneous performance of the SMC-E. Since energy is exchanged between the highest voltage cell and

lowest voltage cell directly, the equalization speed is high from the beginning. The slew rate of voltage equalization of the SMC-E under three cases are $51.67mv/h$, $50mv/h$, and $32.5mv/h$, respectively. When the voltage level of two higher-level cells or two lower-level cells becomes almost equal to each other, the switching pattern is alternately changed to maintain the equalization between them. Furthermore, the balancing current is reduced since the voltage deviation between the cells decrease. Vividly, the performance of the SMC-E follows the mechanism, described in Fig. 3.11 of Section 3.2.2. Therefore, it verifies the theoretical operation principle of the SMC-E. In addition, the final average voltage of the cells is lower than the initial average voltage level. From the experimental results, the voltage drop after the equalizing process is approximately $20mV$.

2.4 Conclusion of the Chapter

This chapter introduced a step-by-step development and design of the SMC-E to mitigate the cell-inconsistency. Based on the theoretical analysis, the switching frequency and balancing capacitance are selected for the fast equalization speed with a consideration of the power loss reduction. In addition, the design considerations for the balancing capacitance, the switch-matrix structure with the gate driving methods, and the current sensing scheme are discussed.

The performance of the SMC-E is verified by hardware experiments. In all test scenarios, the SMC-E always show a high performance in terms of equalization capability, equalization-speed, and stability. The optimal pairing algorithm performs effectively to overcome the impact of the initial distribution scenarios.

Chapter 3

Novel Simulation Techniques for the Performance Assessment of SET-E in Long-term Operation

Since various equalizer topologies have been introduced in recent years, choosing a suitable equalizer for the cell level is difficult. For a fair comparison, the equalizer hardware need to be made and implemented for the same battery string under the same homogeneous conditions. However, the hardware-based comparison requires a lot of investment and time, which slows down the development process. Furthermore, it is not guaranteed that the homogeneous conditions can be achieved in all test scenarios due to their material tolerance. Thus, simulation-based comparisons are more attractive. In this chapter, two effective performance assessments are introduced to compare the performance equalizer during entire equalizing process.

3.1 Real Time Simulation System

3.1.1 RTSS Platform

Among the active balancing methods in the generative energy schemes, the switched-energy-tank equalizers (SET-E) have many advantages. The most popular SET-Es are the switched-inductor equalizer (SI-E), the switched-capacitor equalizer (SC-E), the switched-resonance equalizer (SR-E), and the switch-matrix capacitor equalizer (SMC-E). In all variants of SET-E, their energy exchange is based on the charge transfer operation between the cells and an energy tank as the carrier. In addition, the operation of the SET-Es requires a high switching frequency to achieve high performance. Furthermore, the equalizing process is long because the equalizing current is much lower than 1C-rate of the cells. Therefore, the conventional simulation tools such as PSIM, Plecs, and Matlab requires a long execution time to finish the long-term operation of the equalizers due to the limited computation capability and memory of the PC.

To overcome the inherent limitation, the capacity of the cells can be scaled down many times with the aim of reducing the execution time. However, the capacity scaling down also changes the open-circuit-voltage (OCV) versus SOC characteristic of the cells, which makes the operation of the SET-Es different. For illustrative purposes, the simulation results of the SC-E under two scenarios, including the original capacity setting and the 10 times scaled-down case, are shown in Fig. 3.1. In this test, the circuit and operation parameters are set to be the same in both scenarios. It is clear that this capacity scaled-down significantly reduces the equalizing current, and thus, it changes the result of the entire equalizing process. Thus, it is necessary to transform the simulation results of the scaled-down case to that of the original model.

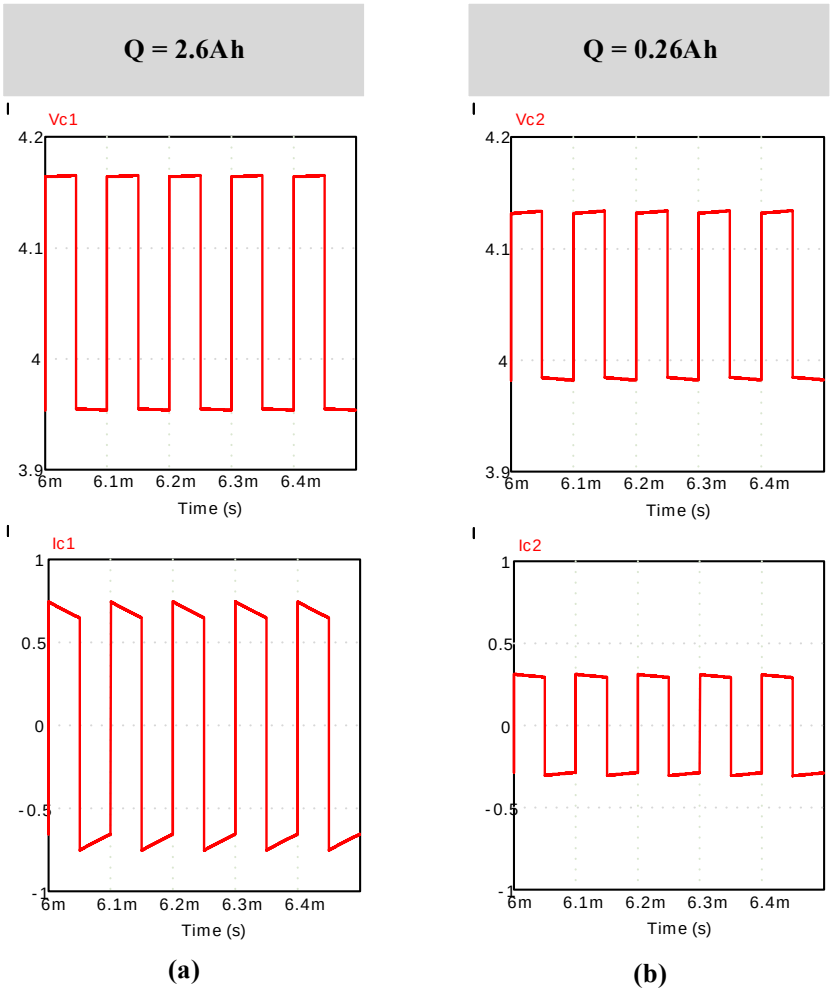


Fig. 3.1 Voltage and current of the SC-E during: Original capacity setting; (b) 10 times scaled-down of capacity.

On the other hand, the real-time simulation (RTSS) based on the hardware-in-the-loop (HIL) equipment such as Typhoon HIL, RT-Box, or OPAL-RT is the viable alternative [86, 25, 87]. With a strong computation capability, the RTSS can simulate the switching model of the SET-Es accurately and no capacity scaled-down is required. In this thesis, the battery model and the SMC-E are implemented by a RTSS (Typhoon HIL 602+).

By virtue of high computational capability, the RTSS can emulate the switching model of the equalizer directly as in Fig. 3.2(a). The existing model of battery cell on RTSS provides

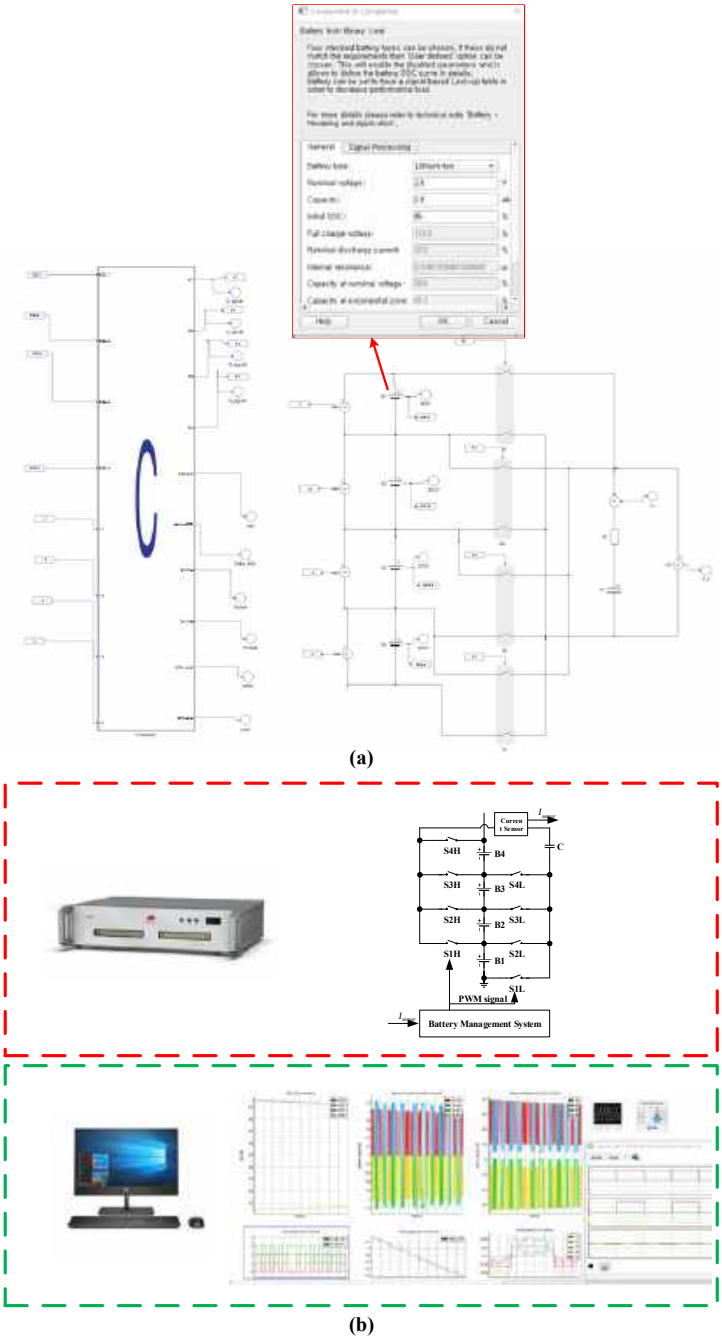


Fig. 3.2 RTSS platform setting: (a) Circuit model on RTSS; (b) SCADA platform for result monitoring.

various models with customization feasibility. Thus, various test scenarios can be set for the performance comparison. In addition, various equalizing strategies can be embedded in the C-function block. After the model is downloaded to the HIL, the SCADA platform on RTSS

Table 3.1 EXPERIMENTAL RESULTS vs. HIL RESULTS-BATTERY VOLTAGES (mV)

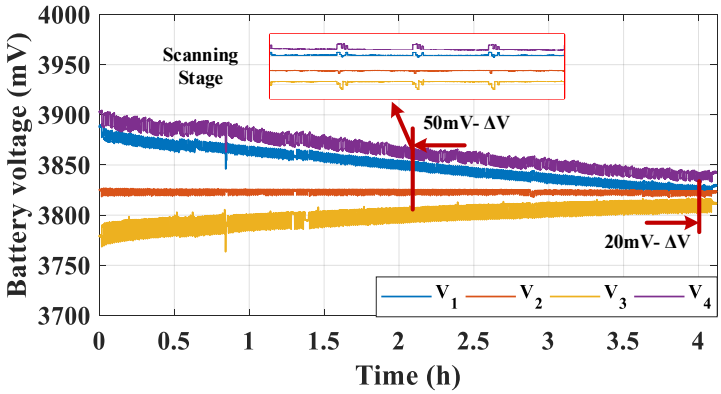
	#1	#2	#3	#4	ΔV
Initial	3898	3825	3760	3912	152
Exp.	3823	3823	3814	3844	20
HIL 4 cells	3826	3823	3820	3839	19

provides a real-time visualization of the test results. The test results including cell voltages, SOC level, operating current, and calculated parameters can be recorded for illustration in a future process. During the real-time operation, the operating mode and operating setting can be changed for the test of hot-swap scenarios or the test of fault conditions.

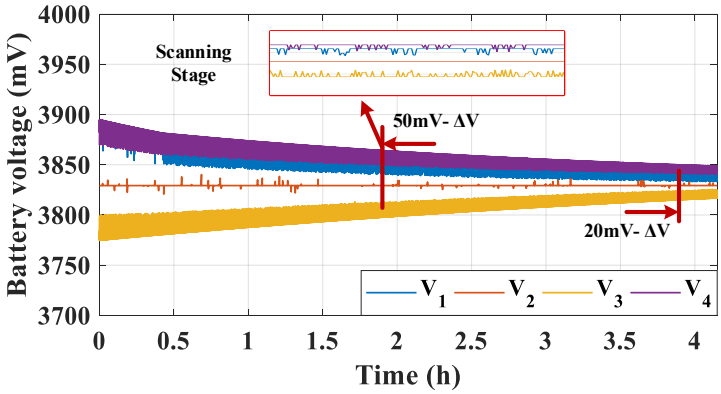
3.1.2 Performance Verification

The RTSS can be implemented to verify the performance of the equalizer in real-time. First of all, the accuracy of the battery model and the design of the equalizer can be assessed by comparing the hardware experimental results with the results on RTSS. Both hardware-based experiments and RTSS tests occurred under the same initial conditions, which are summarized in Table 3.1. The circuit parameters of the SMC-E are similar to that of the design in Chapter 2. The recorded voltage profiles from the hardware experiments and RTSS tests are illustrated in Fig. 3.3 for comparison. Vividly, the voltage profiles in the two platforms are nearly similar to each other since the model on RTSS and the actual characteristic of the hardware are the same. Thus, RTSS-based simulations can be utilized to assess the performance of the equalizers.

Furthermore, the RTSS provides a customization feasibility in terms of circuit design and initial condition of the battery cells. Thus, the equalizers can be tested under various test scenarios with a fair comparison. For example, the same SMC-E is implemented for 6S1P



(a)

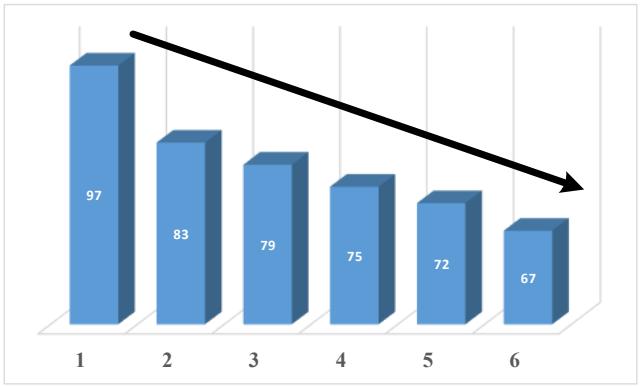


(b)

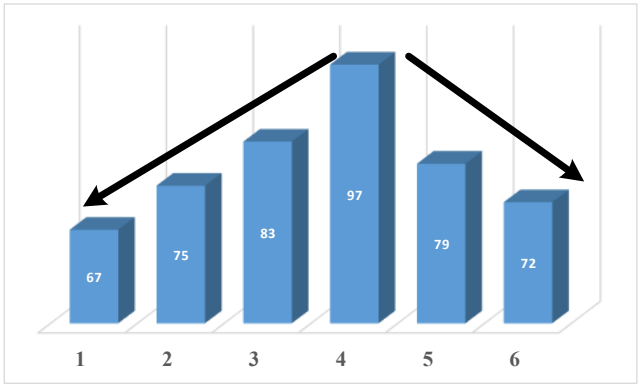
Fig. 3.3 Voltage profile comparison: (a) the experimental results; (b) HIL test for 4 cells.

battery string in three different scenarios, where the initial energy of the cells is distributed in descending order (scenario #1), convex order (scenario #2), and concave order (scenario #3) as in Fig. 3.4.

The corresponding SOC and voltage profiles of the cells under three scenarios are illustrated to assess the performance of the SMC-E. It is observed that the performance of the SMC-E unit is similar under different energy distributions. Although the SMC-E unit in 6S1P cells requires a longer equalization time than in the 4S1P cells, the time increment to achieve 10% SOC deviation or $100mV$ voltage deviation is small. Thus, the influence of cell numbers



(a)



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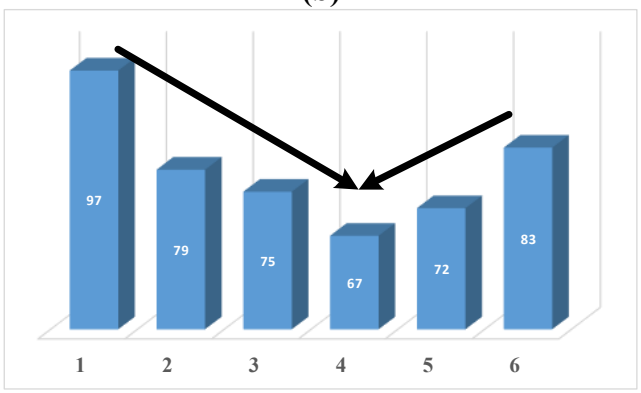


(c)

Fig. 3.4 Initial energy distribution: (a) Scenario #1: Descending order; (b) Scenario #2: Convex order; (c) Scenario #3: Concave order.

on the performance of SMC-E is weak. Based on the operating profiles, the performance indices of the SMC-E are calculated and summarized in Table 3.2. It is observed that the performance indices of the SMC-E are high in all test scenarios where the *DoSE* is higher

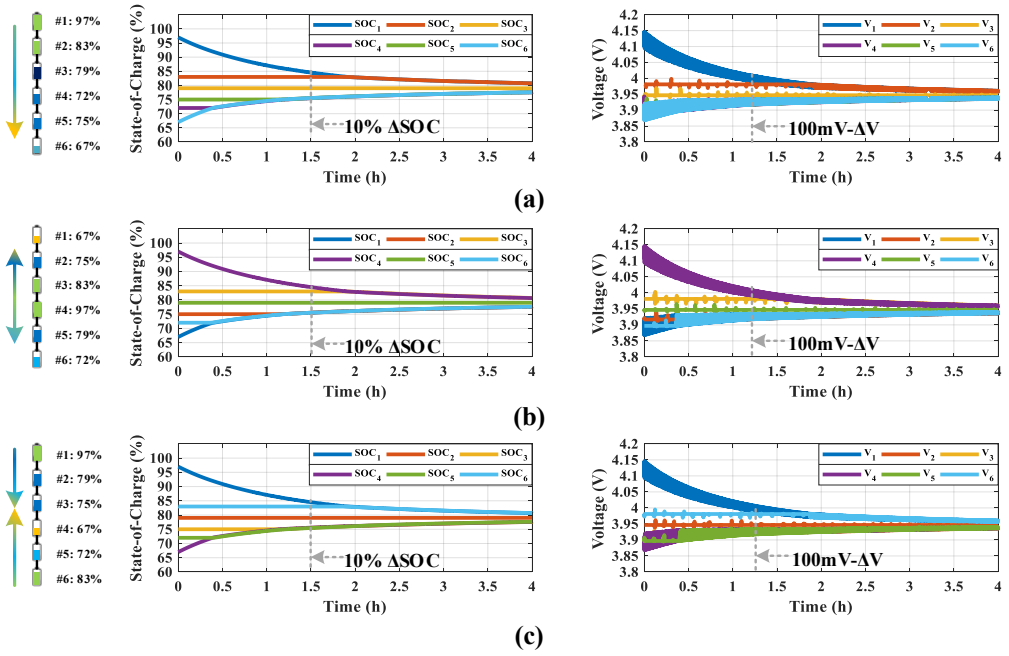


Fig. 3.5 SOC and Voltage profiles of the cells in: (a) Scenario #1; (b) Scenario #2; (c) Scenario #3.

Table 3.2 SUMMARY OF PERFORMANCE INDICES

	$DoSE[\%]$	$DoVE[\%]$	$SR_{SOC}[\%/h]$	$SR_V[mV/h]$	*Charge transfer scheme*	*Additional sensing*	*Initial voltage distribution dependency*
SMC-E	$89 \sim 90.6$	$92.3 \sim 93$	$17.3 \sim 18.1$	$154.7 \sim 178$	**Direct 1-to-1**	**One current sensor**	**Weak**

*N: number of series connection;

than 89%, DoVE is higher than 92.3%, and the slew rate of SOC and voltage are over $17.3\%/h$ and $154.7mV/h$, respectively. It means that the SMC-E unit can effectively mitigates the inconsistency for cell-level in the battery system.

Furthermore, the RTSS can be used to assess the performance of the SMC-E in non-IDLE mode. The same design of the SMC-E is implemented for a 4S1P battery string (3.6V-2.9Ah) and the SMC-E is activated while the cells are simultaneously cycled by a sequence as in Fig. 3.6. The cell voltages, SOC levels, and operating current profiles are illustrated in Fig. 3.7. Vividly, the equalization process is executed simultaneously with the cycling process.

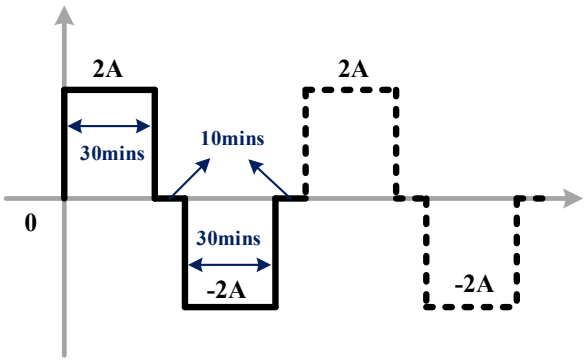


Fig. 3.6 Cycling sequence for 4S1P cell string.

After 3 cycles, the cell voltages are equalized within 50mV of voltage deviation and 4% of SOC difference. However, the cooperation between the cycling process and the equalization process should be carefully monitored to prevent the overload condition for the cells. The current profiles in Fig. 3.7 (c) show a high operation current of cell #1 and #4 in the first cycle due to their high equalizing currents.

In summary, the RTSS is a powerful evaluation platform to verify the design and the performance of the equalizers. When the model on RTSS is similar to the actual hardware, the equalization process can be emulated with high accuracy. In addition, various data can be recorded during the equalization of the RTSS, and thus, more evaluation criteria can be assessed.

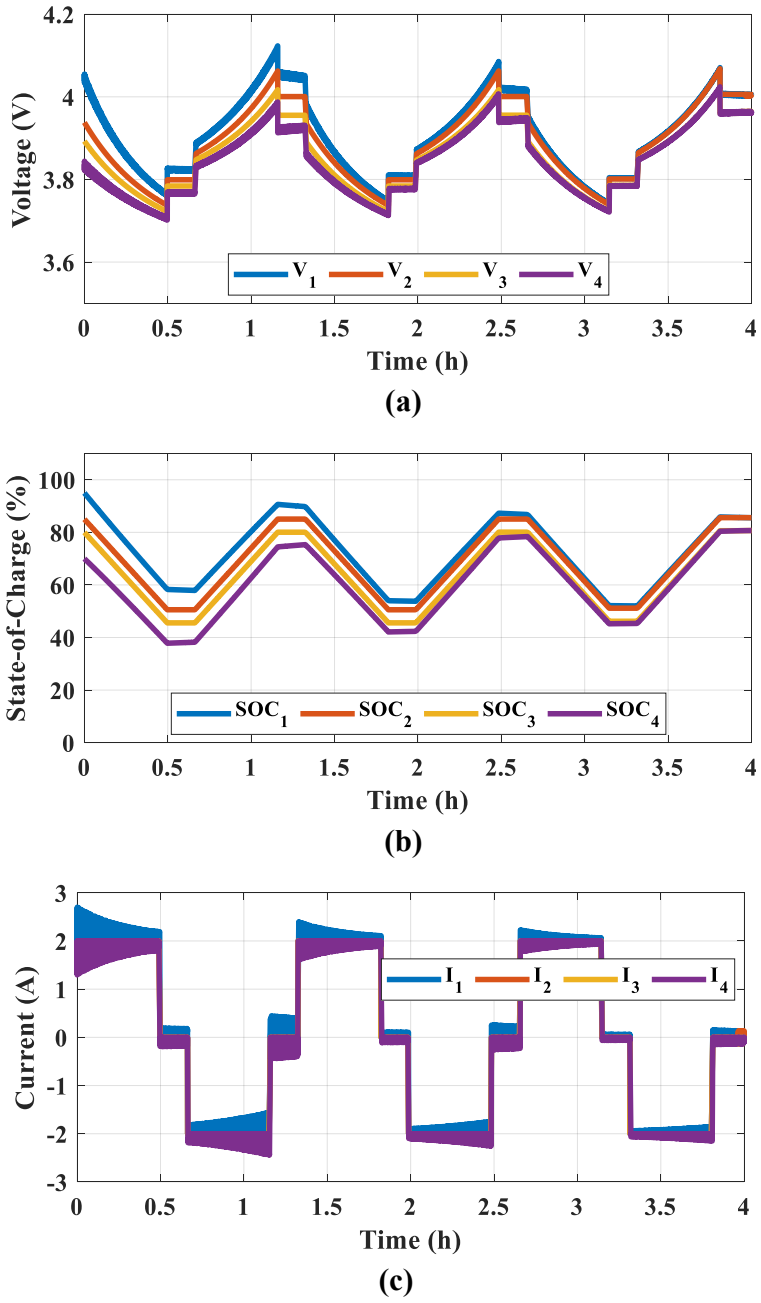


Fig. 3.7 Operation profiles of the cells during cycling process: (a) voltage profiles, (b) SOC profiles, (c) current profiles.

3.2 Unified Average Model based Simulation

Although the RTSS based simulations have high accuracy and performance, the RTSS is expensive and has a limited computation core. Furthermore, a second execution time in RTSS reflects a second in the real process, and thus, the execution time of the RTSS for the long-term operation takes a lot of time. Imagine that a $1A$ constant current equalizes $100Ah$ battery cells, days of execution time are required to finish a single process, and more time is essential for the multiple test scenarios. That's why an alternative simulation method that can simulate the long-term operation of the equalizer with a short execution time is essential.

From the perspective of the power electronics, the switching operation can be replaced by the average models for the simulation of the long-term operation [88]. Furthermore, the topological configuration that have a similar operating principle will have the same average model. Although the conventional studies of the dedicated models for the individual topology exist, a versatile average model should be developed to fairly compare their performance under different scenarios with a fast execution time. In this Section, a unified average model (UA-model) is proposed to emulate the equalization process of the switched energy tank equalizers (SET-Es). The UA-model can be used to compare the equalization performance as well as verify the design of the equalizers in a short time.

3.2.1 UA-model: Operating Principle

In this section, four equalizer configurations are considered, including the SI-E, the SC-E, the SR-E, and the SMC-E as shown in Fig. 3.8. The performance comparison between the equalizers aims to derive the suitable topological configuration or design of the equalizers. Even if the circuit configurations of the equalizer are different, their energy exchange follows

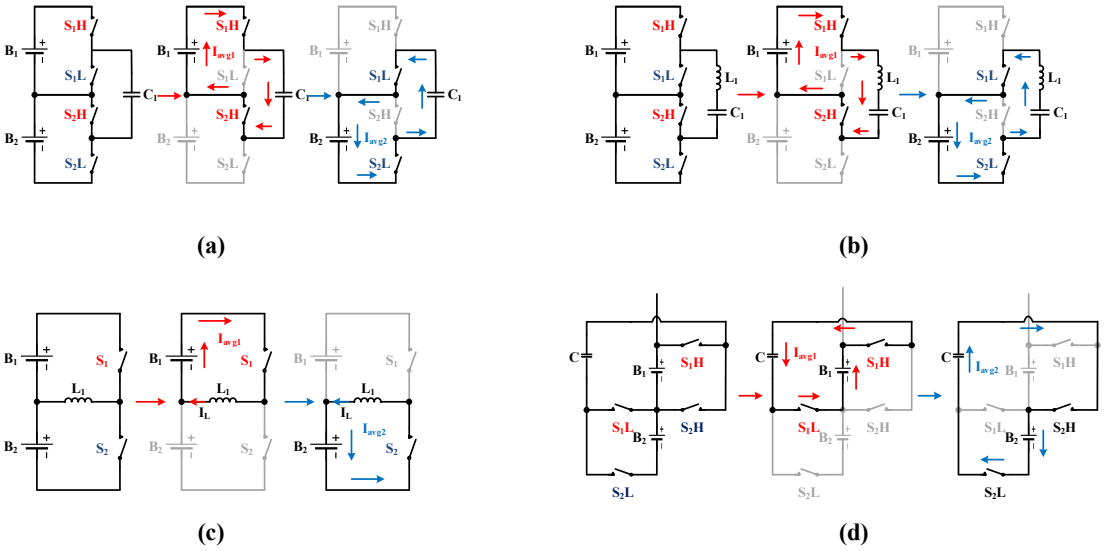


Fig. 3.8 Operating principle of various equalizers: (a) SC-E, (b) SR-E, (c) SI-E, (d) SMC-E.

the same scheme. Assuming that the cell $\#B_1$ has a higher energy level than the cell $\#B_2$, an equalization cycle is divided into two phases.

• Phase A: in Fig. 3.8(a), (b), and (c), the switches S_1H and S_2H are turned on, and thus, the energy tank is charged from $\#B_1$. By the same token, the switches S_1H and S_1L are activated for the SMC-E as in Fig. 3.8(d). In the sense of average, the energy tank is charged by an average equalization current, I_{avg1}.

• Phase B: the switching pattern is inverted to transfer the energy from the energy tank to cell $\#B_2$. In Fig. 3.8(a), (b), and (c), the switches S_1L and S_2L are activated while the other switches are turned off. Similarly, the switches S_2H and S_2L of the SMC-E in Fig. 3.8(d) are turned on to do the same task. Approximately, cell $\#B_2$ is charged by an average current, I_{avg2}.

By repeating the process, the energy is gradually transferred from the high-voltage cell to the low-voltage cell. Energy can be exchanged autonomously or is governed by the control algorithm.

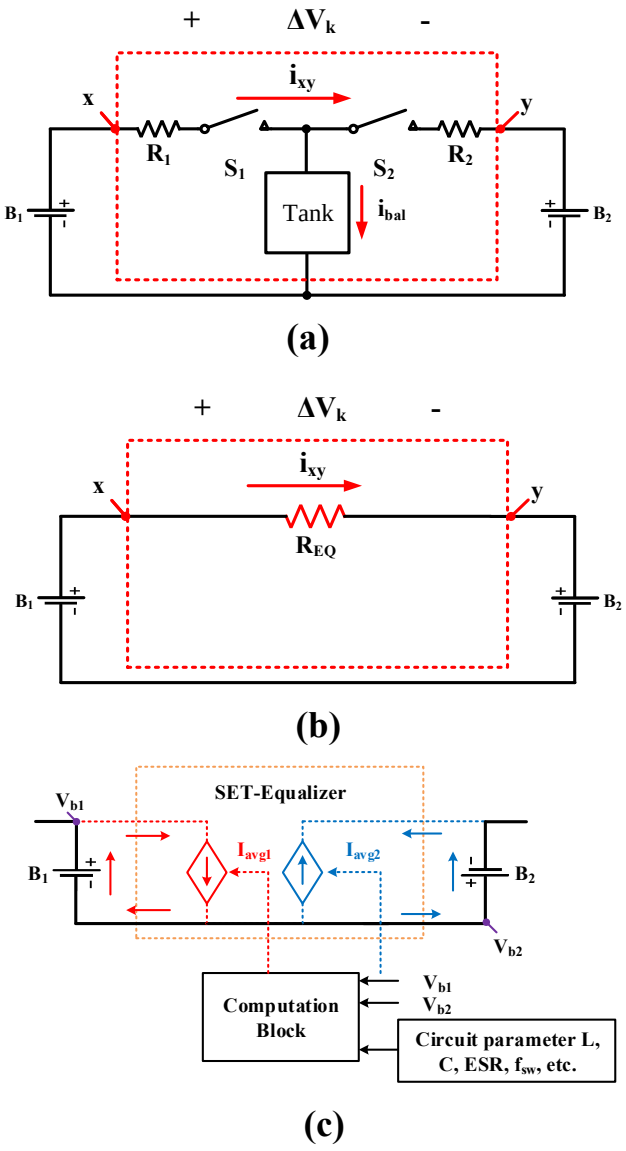


Fig. 3.9 Average model evolution of SET-Es: (a) Equivalent circuit based on the operation principle, (b) Conventional equivalent resistance model, (c) UA-model.

The operating principle of the equalizers can be represented by the equivalent circuit as in Fig. 3.9(a). Typically, the loss model of the switched-energy-tank converter is analyzed. Based on the approximate loss model [89, 90], the SET-E can be emulated by an equivalent resistance, R_{EQ}, as Fig. 3.9(b) [91, 92]. In the R_{EQ} model, the equalizing current is calculated

based voltage difference between two cells. However, since the balancing process of SET-Es has a non-linear characteristics, the equivalent resistance model fails to accurately reflect the balancing process. Thus, the simulation results become dissimilar to the actual results. In fact, the equalization is performed by the amount of charge that flows into or out of two cells. In the UA-model shown in Fig. 3.9(c), two controlled-current sources are utilized to emulate the energy exchange.

The main idea of the UA-model is to identify the average amount of charge that flows into or out of the cell during the equalization process. The average current is formulated for various balancing schemes as follows.

3.2.1.a Switched-Capacitor Equalizer (SC-E) and SMC-E

In Section 2.1.1 of Chapter 2, the operating principle of the SC-E and the SMC-E was analyzed. According to the analysis, the average current of the cells are expressed as

$$I_{avg1} = \frac{1}{2} C f_{sw} \left(V_{B1} - V_{B2}\right) \left(1 - exp(\frac{-D_1}{f_{sw} R_1 C})\right), \tag{3.1}$$

$$I_{avg2} = \frac{1}{2} C f_{sw} \left(V_{B2} - V_{B1}\right) \left(1 - exp(\frac{-D_2}{f_{sw} R_2 C})\right) exp(\frac{-1}{2 f_{sw} R_2 C}). \tag{3.2}$$

By applying (3.1) and (3.2) to the UA-model in Fig. 3.9(c), the equalizing process is emulated. In addition, the direction of the equalization currents, I_{avg1} and I_{avg2}, is decided by the voltage difference between the two cells. Therefore, the cell #1 is discharged by I_{avg1} while the cell #2 is charged by I_{avg2}, and thus, the energy levels of the cells are equalized after multiple equalizing cycles. The voltages of the cells are continuously monitored to adjust the amplitude and the direction of the average equalizing currents.

3.2.1.b Switched-Resonant Equalizer (SR-E)

Because the inherent disadvantages of the SC-E and the SMC-E are bulky volume and loss of the circuit, the SR-E can be a promising solution. Only one additional inductor is connected to the equalizing capacitor in series for the resonant operation. Because the switching pattern is the same, the charge transfer process is similar to the SC-E. Denote that the damped resonant frequency of the m-th cell is

$$\omega_{rk} = \sqrt{\frac{1}{LC} - \beta_k^2}, \tag{3.3}$$

where $\beta_k = \dfrac{R_k}{2L}$ is the dissipation factor and R_k is the loop resistance with $(k = 1,\ 2)$. Then, the charge income and outcome of the capacitor are calculated by

$$Q_{in} = C\left(V_{B1} - V_{c\_avg}\right)\left(1 + exp(\frac{-\beta_1\pi}{\omega_{r1}})\right), \tag{3.4}$$

$$Q_{out} = -C\left(V_{c\_avg} - V_{B2}\right)\left(1 + exp(\frac{-\beta_2\pi}{\omega_{r2}})\right). \tag{3.5}$$

By the same token with the SC-E and the SMC-E, the average equalizing currents of the cells are expressed by

$$I_{avg1} = \frac{1}{2}Cf_{sw}\left(V_{B1} - V_{B2}\right)\left(1 + exp(\frac{-\beta_1\pi}{\omega_{r1}})\right), \tag{3.6}$$

$$I_{avg2} = \frac{1}{2}Cf_{sw}\left(V_{B2} - V_{B1}\right)\left(1 + exp(\frac{-\beta_2\pi}{\omega_{r2}})\right). \tag{3.7}$$

3.2.1.c Switched-Inductor Equalizer (SI-E)

In the SI-E, the equalizer operates as a buck-boost converter. Various theoretical analysis have been reported [46, 47]. In this thesis, the analysis is inherited and is summarized as

Table 3.3 AVERAGE EQUALIZING CURRENT CALCULATION FOR UA-MODEL

Topology	Key formula
SC-E & **SMC-E**	$I_{avg1} = \frac{1}{2}Cf_{sw}(V_{B1} - V_{B2})\left(1 - exp(\frac{-D_1}{f_{sw}R_1C})\right)$ $I_{avg2} = \frac{1}{2}Cf_{sw}(V_{B2} - V_{B1})\left(1 - exp(\frac{-D_2}{f_{sw}R_2C})\right)exp(\frac{-1}{2f_{sw}R_2C})$
SR-E	$I_{avg1} = \frac{1}{2}Cf_{sw}(V_{B1} - V_{B2})\left(1 + exp(\frac{-\beta_1\pi}{\omega_{r1}})\right)$ $I_{avg2} = \frac{1}{2}Cf_{sw}(V_{B2} - V_{B1})\left(1 + exp(\frac{-\beta_2\pi}{\omega_{r2}})\right)$
SI-E	$I_L = \frac{DV_{b1} - (1-D)V_{b2}}{D^2(R_1+R_L) + (1-D)^2(R_2+R_L)}$ $I_{avg1} = DI_L$ $I_{avg2} = -(1-D)I_L$

follows:

$$I_L = \frac{DV_{b1} - (1-D)V_{b2}}{D^2(R_1+R_L) + (1-D)^2(R_2+R_L)}, \tag{3.8}$$

where D is the duty ratio of phase A; R_1 and R_2 are the loop resistance; R_L is the equivalent series resistance of the inductor. Therefore, the equalization currents of two cells are respectively calculated by

$$I_{avg1} = DI_L, \tag{3.9}$$

$$I_{avg2} = -(1-D)I_L. \tag{3.10}$$

For a comparison, the average equalizing current of the equalizers are summarized in Table 3.3.

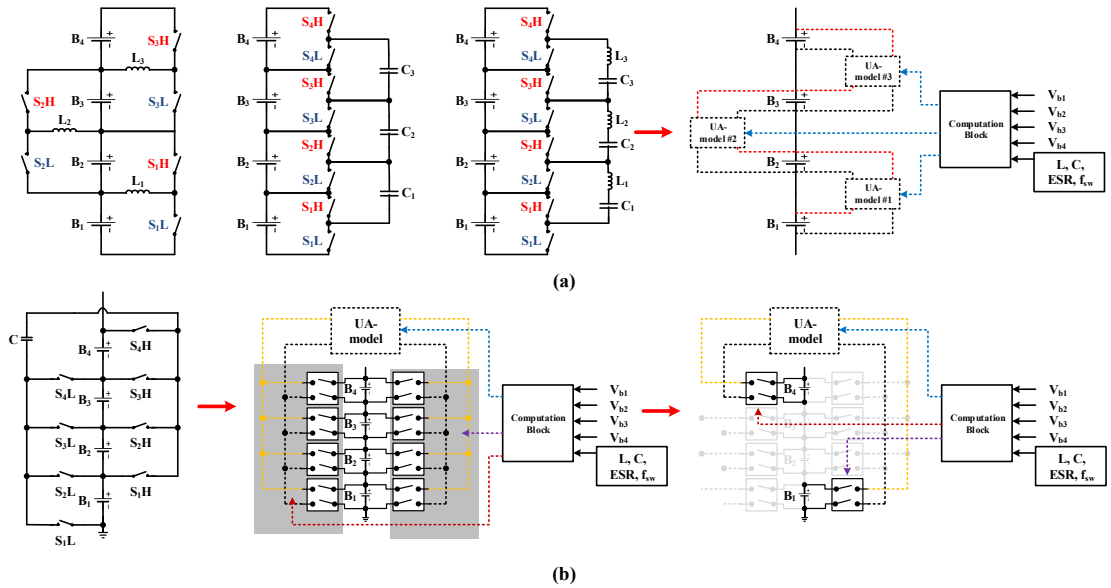


Fig. 3.10 Implementation of UA-model: (a) autonomous SET-E type; (b) governed switch-matrix type (SMC-E).

3.2.2 Performance Comparison by UA-model

Since an UA-model reflects the energy exchange between two cells, the topological configuration and control method will decide the amount of the UA-models to be employed in the simulation. For an instant, the two configuration types of UA-model are implemented for two groups of topology as in Fig. 3.10. For the SI-E, the SC-E, and the SR-E as shown in Fig. 3.10(a), where the switches are autonomously controlled by a pair of complementary PWM signals. Since energy is only exchanged between two adjacent cells, (N-1) UA-models are utilized to re-present the equalization of N series cells. The battery voltages are continuously monitored to adjust the average equalizing currents of the UA-models.

Furthermore, the SMC-E only requires an UA-model as shown in Fig. 3.10(b). The switch-matrix in the actual circuit is transformed into a network of double-pole double-throw (DPDT) switches, which is utilized to connect the highest-voltage cell and the lowest-voltage

Table 3.4 CIRCUIT PARAMETER SETTING

Topology	SI-E	SC-E	SR-E	SMC-E
Circuitry Parameters	$f_{sw} = 20\ kHz$ $L = 400\ \mu H$ $R_1 = R_2 = 0.15\ \Omega$ $D_1 = D_2 = 0.45$	$f_{sw} = 20\ kHz$ $C = 2200\ \mu F$ $R_1 = R_2 = 0.15\ \Omega$ $D_1 = D_2 = 0.45$	$f_{sw} = 15\ kHz$ $C = 200\ \mu F$ $L = 0.47\ \mu H$ $R_1 = R_2 = 0.15\ \Omega$ $D_1 = D_2 = 0.45$	$f_{sw} = 20\ kHz$ $C = 2200\ \mu F$ $R_1 = R_2 = 0.15\ \Omega$ $D_1 = D_2 = 0.45$
Initial SOC	$SOC_{1,\ 2,\ 3,\ 4} = 70,\ 80,\ 95,\ 85$ [%]			

cell to the UA-model. For illustrative purposes, if the DPDT of cell #1 and cell #4 are triggered while the others are kept off, cell #1 and cell #4 are connected to two ports of the UA-model. Next, the computation block sends the calculated average equalizing currents to the UA-model. After a duration, the computation block scans the cell voltages again to decide the switching pattern of the DPDT network as well as the average equalizing current. When the voltage of the cell #1 and the cell #4 are lower than the other cells, the switching pattern of the DPDT network changes. Thus, the energy of all cells is gradually equalized.

By implementing the UA-model for the equalizers, their performance can be tested and compared. In this test, the target system is a 4S1P battery string (18650 NMC cell 3.6V/2.6Ah), and three types of simulation models are compared, including switching model on RTSS, R_{EQ} based model, and UA-model on PSIM, respectively. It is noted that the switching model can be implemented either by RTSS or by PSIM. However, the switching model in PSIM is too slow to be computed. In all test, the circuit parameters of the equalizers are summarized in Table 3.4. Considering the inherent speed difference, the total simulation time is set at 2 hours for the SI-E, and at 3 hours for the others, respectively. The performance of the equalizers will be assessed by the evaluation criteria in Section 1.6 of Chapter 1.

To verify the accuracy of the UA-model, the initial SOC levels of the cells are set as Table 3.4. The cell voltage, SOC level, and equalizing current profiles are illustrated in

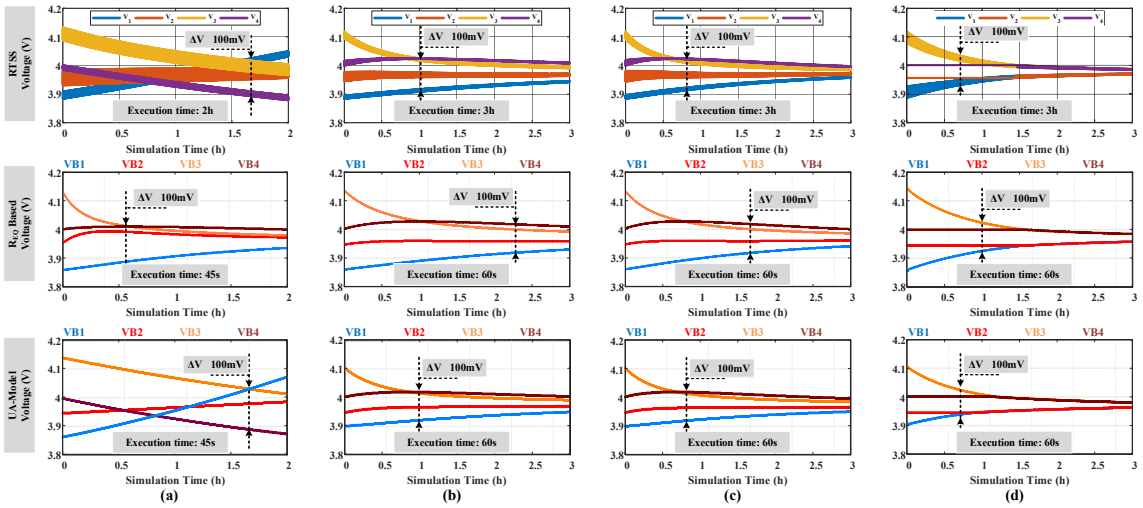


Fig. 3.11 Voltage profiles of the cells during the equalization by RTSS, R_{EQ} model, and UA-model: (a) SI-E; (b) SC-E; (c) SR-E; and (d) SMC-E.

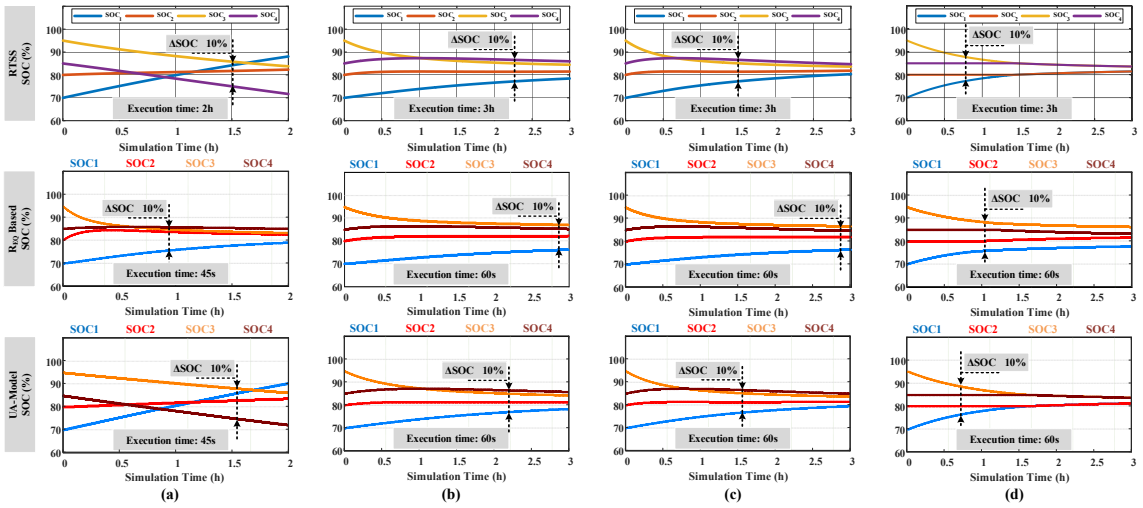


Fig. 3.12 SOC profiles of the cells during the equalization by RTSS, R_{EQ} model, and UA-model: (a) SI-E; (b) SC-E; (c) SR-E; and (d) SMC-E.

Fig. 3.11, Fig. 3.12, and Fig. 3.13, respectively. Vividly, the R_{EQ} model fails to emulate the equalization of the SI-E, and the operating profiles are different from the other profiles. R_{EQ} model also shows an incorrect simulation for the other equalizers (SC-E, SR-E, and SMC-E). In contrast, the equalization profiles show a similar behavior and performance of the equalizers between the UA-model and the switching model on RTSS. The voltage deviation

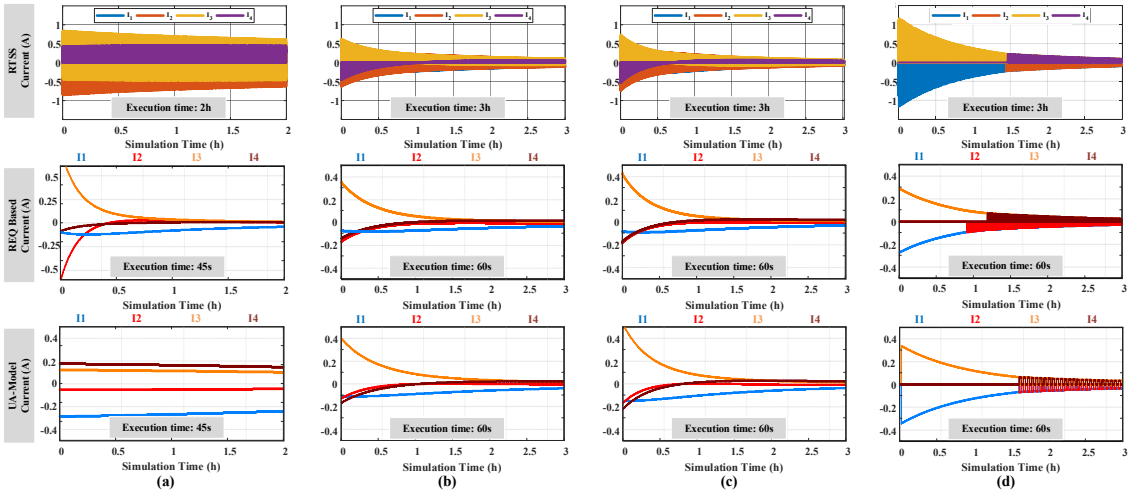


Fig. 3.13 Current profiles of the cells during the equalization by RTSS, R_{EQ} model, and UA-model: (a) SI-E; (b) SC-E; (c) SR-E; and (d) SMC-E.

and SOC deviation by the RTSS and UA-model in Fig. 3.11, Fig. 3.12, and Fig. 3.13, are so similar that verifies the accuracy of the UA-models. Although the equalizing currents in the UA-model only represent the average value of the switching waveform from the RTSS, the current profiles from both simulations match each other. Thus, the theoretical operating principle of the equalizers can be verified by the UA-model. It should be observed that the UA-model requires only about 60 s to simulate 3 h of the overall process, while the RTSS needs exactly 3 h to perform the same task. By this means, the UA-model can evaluate the equalizer performance with an accelerated speed and high accuracy.

Since the accuracy of the UA-model is verified, more test scenarios are assessed for the equalizers as shown in Fig. 3.14. For the first three scenarios, the number of cells (4S1P) is the same but the energy distribution of the cells is different. This test assesses the performance stability of the equalizer under various energy distributions of the same battery system. Furthermore, the test scenario in Fig. 3.14(d) presents the cell-inconsistency of an 8S1P battery string while the energy level is descending distributed. The cell voltage and SOC

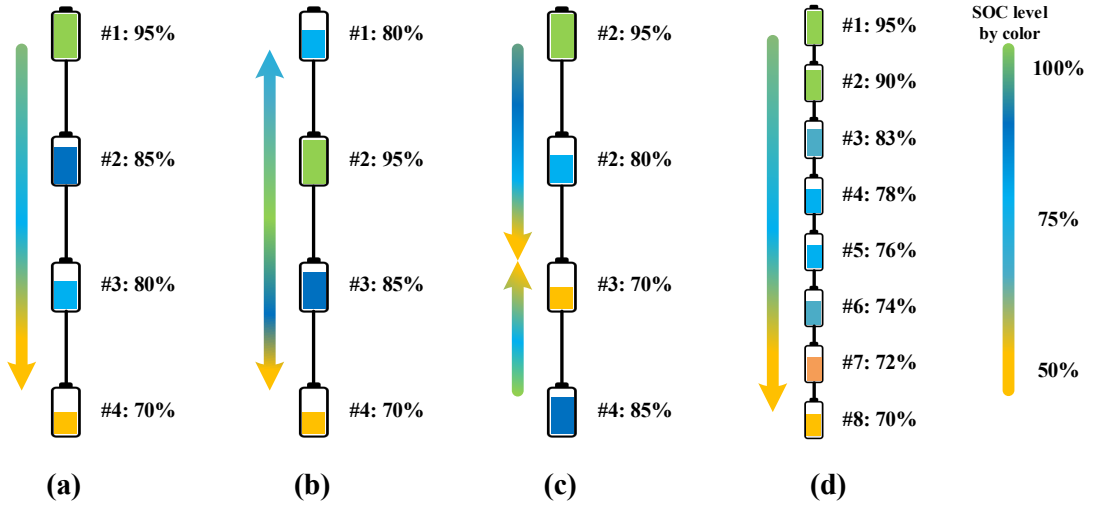


Fig. 3.14 SOC distribution of the cells in various scenarios: (a) Four cells descending; (b) Four cells convex; (c) Four cells concave; (d) Eight cells descending.

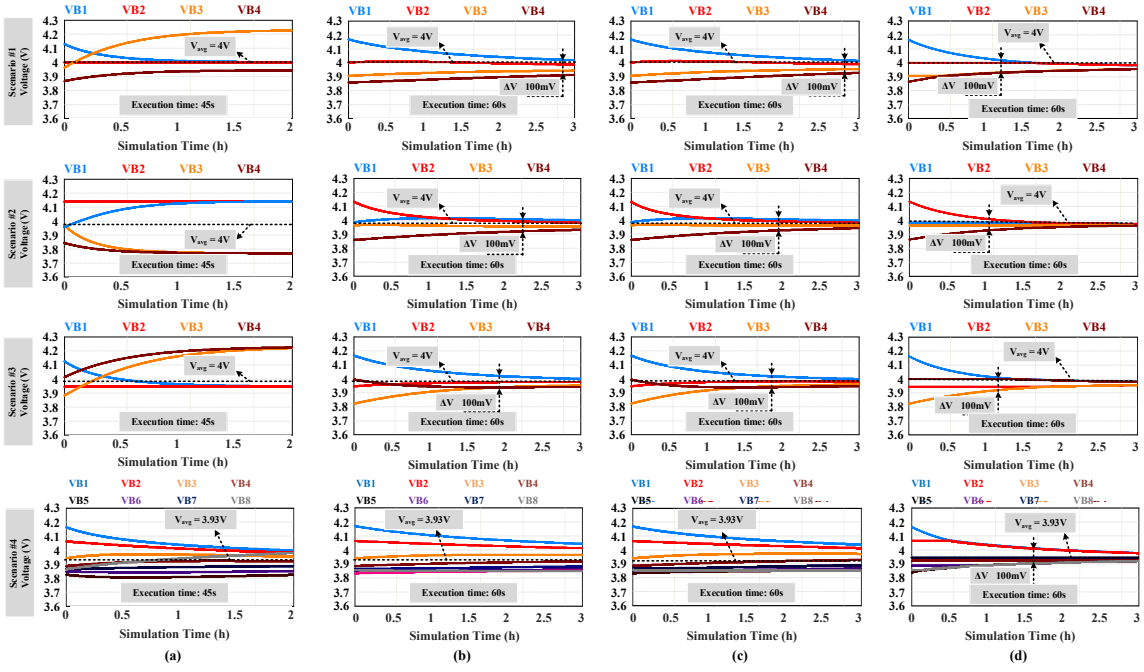


Fig. 3.15 Voltage profiles of the cells during the equalization by RTSS, R_{EQ} model, and UA-model: (a) SI-E; (b) SC-E; (c) SR-E; and (d) SMC-E.

level profiles in all test scenarios are shown in Fig. 3.15 and Fig. 3.16, respectively. Vividly, the SMC-E shows a better performance than the others by virtue of the switch-matrix

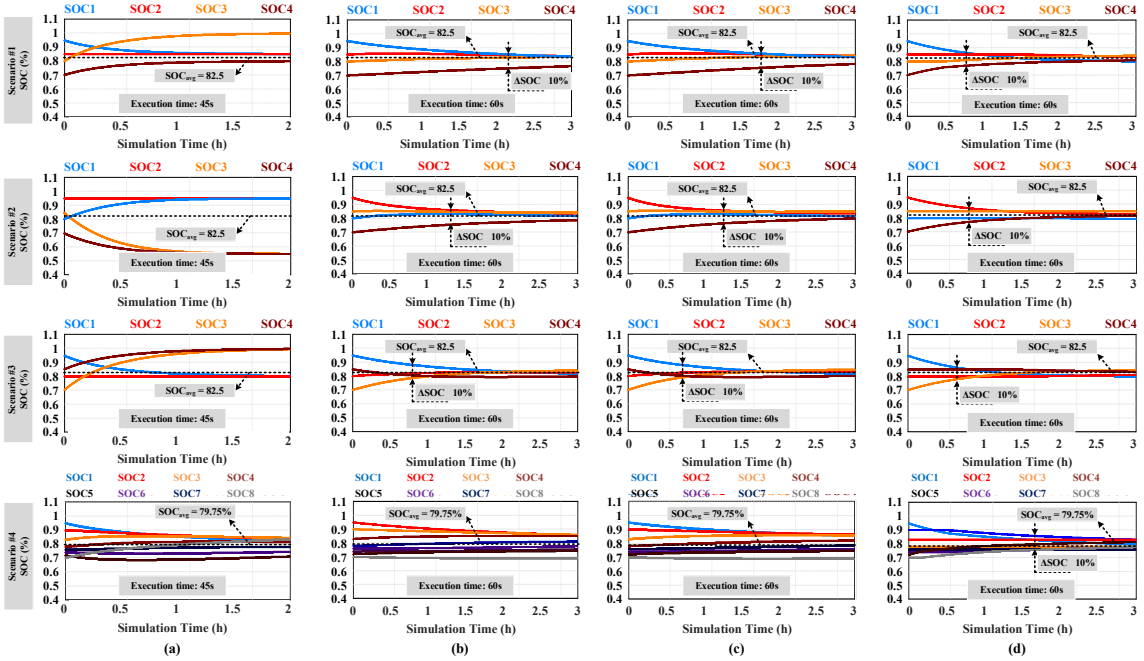


Fig. 3.16 SOC profiles of the cells by UA-model: (a) SI-E; (b) SC-E; (c) SR-E; and (d) SMC-E.

structure, where the cell voltage and SOC levels are equalized over 94 % DoVE and DoSE in all test-scenarios. However, to achieve such a high performance, the proposed SMC-E requires a monitoring circuit to detect the highest voltage and lowest voltage cells. Besides, the number of control signals is also larger than that of the autonomous types. The autonomous single-tier SR-E and SC-E rank in the 2nd and 3rd places with over 80 % DoVE and DoSE indices in test scenarios #1, #2, and #3. However, the performances of the single-tier SC-E and SR-E are significantly reduced in scenario #4, where the number of cells are increased. After 3h, the voltage and SOC levels of the cells are not yet equalized within the required balancing level.

On the other hand, the SI-E shows poor performance under the autonomous control scheme, when the voltage and SOC deviations become larger than the initial point. Thus, the SI-E usually requires an extra complex duty-control algorithm. Specifically, the cell voltage

should be monitored to calculate the duty ratio of the switching control signals. However, the DoVE and DoSE are different from each other due to the polarization effect. Thus, the voltage sensing-based equalization strategy in the SI-E is difficult to guarantee the energy equalization of the cells.

Based on the voltage and SOC profiles, the slew rates are calculated to assess the equalization speed of the equalizers. Because the autonomous control scheme is not suitable for SI-E, its slew rates of voltage and SOC equalization are very low. In the first three scenarios, where only four cells are tested, the SC-E and SR-E show an above-average equalization speed. However, their equalizing speed is not the same in all test scenarios, showing the dependence of the equalization performance on the initial energy distribution. In addition, the equalization speed is significantly reduced when the number of cells is higher. Therefore, the performance stability of the single-tier SC-E and SR-E is poor. In contrast, the SMC-E shows a higher slew rate (>71.67 mV/h SR_V and > 7 %/h SR_{SOC}). Thus, the performance stability of the SMC-E can be maintained even if the number of cells is increased.

Finally, the Coulombic efficiency is calculated from on the SOC profiles of each equalizer. In combination with the other performance indices, the scenario dependency of the equalizers is assessed by the chart in Fig. 3.17. It is clear that the SMC-E shows consistent performance across the test scenarios, where the performance indices are almost the same in all test scenarios as in Fig. 3.17(d). On the other hand, the performance of the other equalizers (single-tier SI-E, SC-E, and SR-E) in all test scenarios are heavily dependent on the initial energy distribution of the cells as well as the number of the cells in the string. For example, the performance of the autonomous single-tier SET-Es shows good performance when the

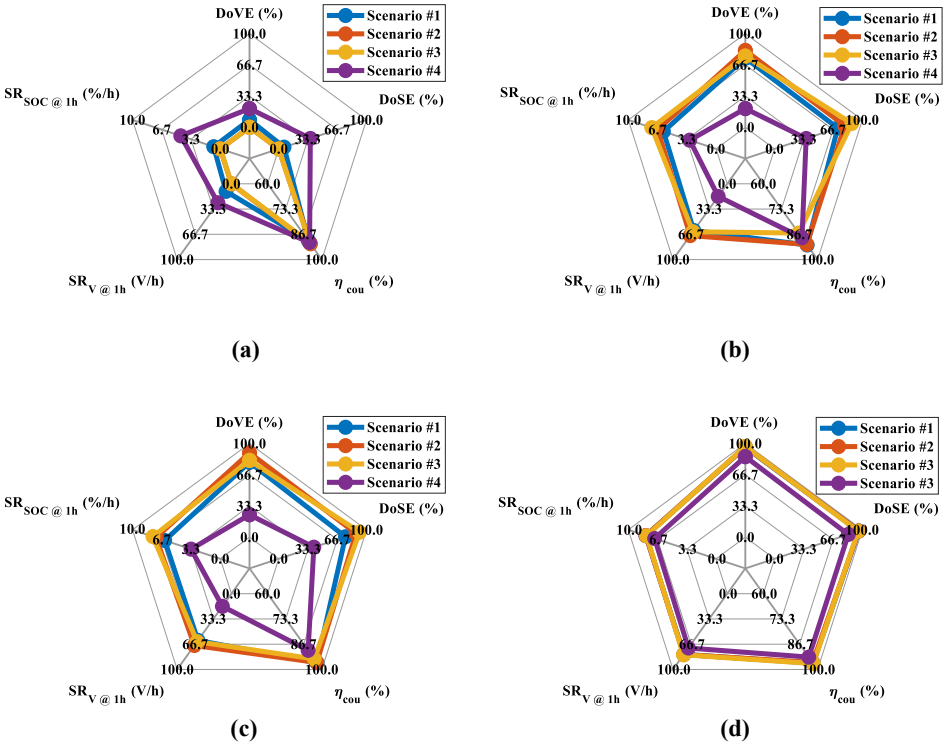


Fig. 3.17 Performance stability under various test scenarios of: (a) SI-E ; (b) SC-E; (c) SR-E; (d) SMC-E.

high-voltage cell and the low-voltage cell are adjacent. In addition, the voltage and SOC profiles in Fig. 3.15 and Fig. 3.16 also reflect the impact of the test scenarios. While the equalization point of the single-tier equalizers (SI-E, SC-E, and SR-E) in all scenarios are dissimilar, the SMC-E shows a consistent performance.

In terms of cost and volume, the SI-E, the SR-E, and the SMC-E require high component counts and volumes. The topological configuration of the single-tier equalizer (SI-E, SC-E, and SR-E) should be improved to overcome the inherent disadvantages. The SMC-E is more

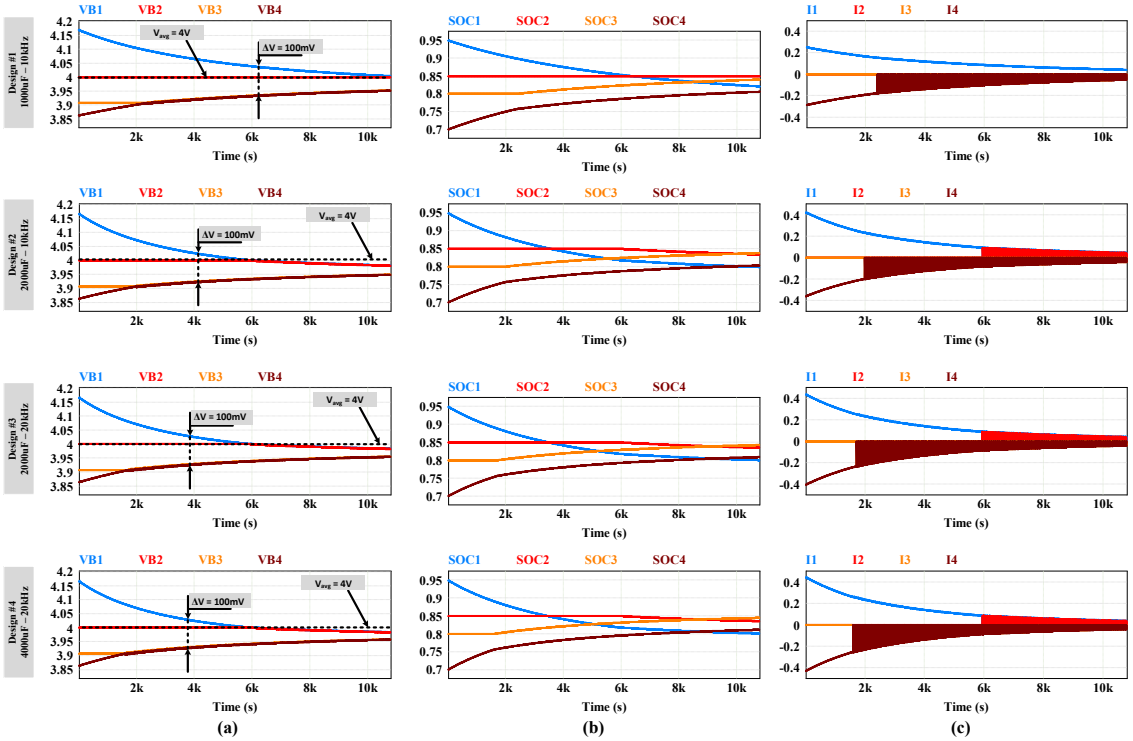


Fig. 3.18 UA-model based performance comparison of various design combination: (a) Voltage profiles; (b) SOC profiles; (b) Current profiles.

promising than the others by virtue of its high equalization capability, high equalization speed, and performance stability.

3.2.3 Design Assessment by UA-model

Since the UA-model can assess the equalization process within a short time. The UA-model can be utilized to verify the designs of the equalizer by executing multiple tests under various scenarios. In Chapter 2, four design combinations of C and f_s are considered, including design $\#1-1000\mu F/10kHz$, design $\#2-2000\mu F/10kHz$, design $\#3-2000\mu F/20kHz$, and design $\#4-4000\mu F/20kHz$. To choose the optimal C and f_s, the simulations based on UA-model are implemented for a 4S1P battery string (18650 NMC 3.6V-2.9Ah). The capacities of the cells are similar but their initial SOC levels are descending as 95%, 85%, 80%, and 70%,

respectively. In every test, the internal resistances of the circuit, R_1 and R_2, are set at 0.15Ω and the duty ratios of the complementary PWM signals, D_1 and D_2, are fixed at 0.45.

The profiles of the cell voltage, the SOC levels, and the equalizing currents in four design combinations are illustrated in Fig. 3.18. Vividly, the design $\#1-1000\mu F/10kHz$ has a lower equalization speed than the other designs, when it requires over 6100s to balance the cell voltage within 100 mV. Furthermore, the designs #2, #3, and #4 show a trivial increment of speed when C and f_s are doubled. In addition, the current profiles in Fig. 3.18(b) describe the same token, where the equalizing process of design #2, #3, and #4 are almost homogeneous. Therefore, increasing C and f_s doesn't accelerate the equalization speed. By considering the equalizing speed and the cost, design $\#3-2000\mu F/20kHz$ is selected.

In summary, the UA-model-based simulation is an effective evaluation method to compare the performance of various topological configurations of the equalizers. Hours of equalization time can be emulated by a UA-model within a few seconds. In addition, the UA-model can be utilized to compare the design options of the equalizer. After that, the design can be assessed again by the switching model on RTSS for better simulation accuracy.

Chapter 4

Switch-Matrix Capacitor Equalizer for Module Equalization

In Chapter 2, the equalization level I is achieved, when the energy levels of the cells inside a module are equalized. However, the mismatch between the modules still exists. Thus, it is essential to have an effective equalizer for the modules, which are connected in series and parallel. Based on the design of the SMC-E, two switches are added to extend the operation of the SMC-E for modular equalization. With the same design, the extended topology can be implemented for both series and parallel connections as in Fig. 4.1. Because the equalization of the modules in series and parallel connections requires a different mechanism, various equalization strategies are proposed for different purposes.

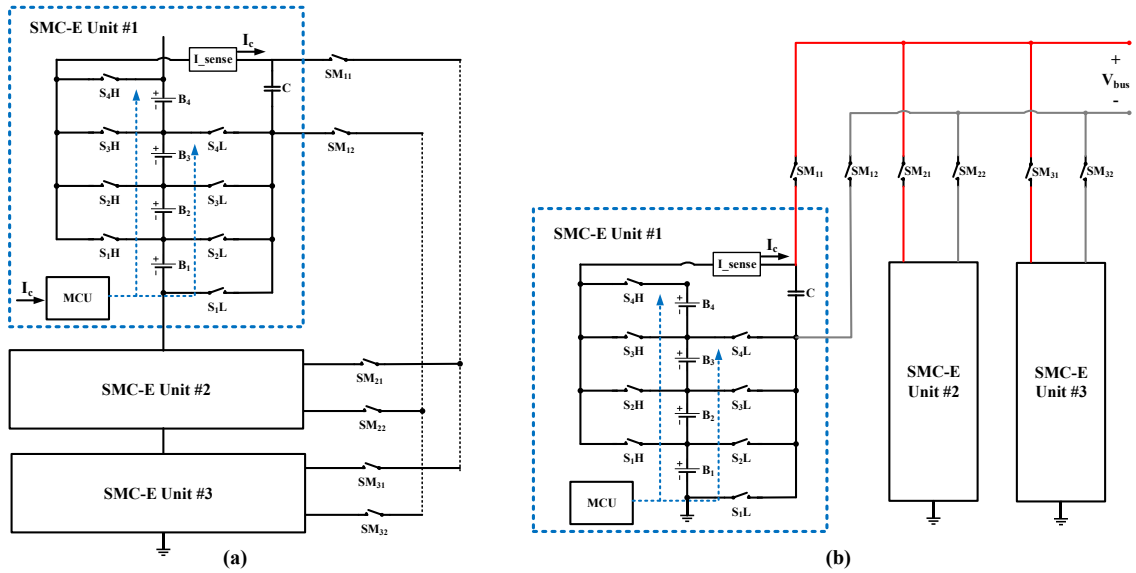


Fig. 4.1 Modular structure of the SMC-E for: (a) Series-connected battery modules; (b) Parallel-connected battery modules.

4.1 Extension of the SMC-E for Series-connected Modules

4.1.1 Use Cases and Conventional Structure

In the EV and a rack of BESS, the modules are connected in series to increase the operating voltage of the system. To mitigate the inconsistency between the cells inside a module, it is recommended to execute the equalization periodically. In this case, the battery rack disconnects from the DC bus to allow the modules to switch to IDLE mode as shown in Fig. 4.2(a). After that the equalizer of the local BMS is triggered to balance the cells inside every module. For the same purpose, the cell equalization is activated for EV before the charging process or at the repair shop as in Fig. 4.2(b). On the other hand, the retired battery pack of EV is directly reused for the second-life battery energy storage system (SL-BESS). Therefore, the energy level of the cells must be equalized and adjusted below 30% of SOC [93].

Since the passive balancing method is widely adopted in the industrial applications, the execution time of the equalization process is long. Although the equalization level I

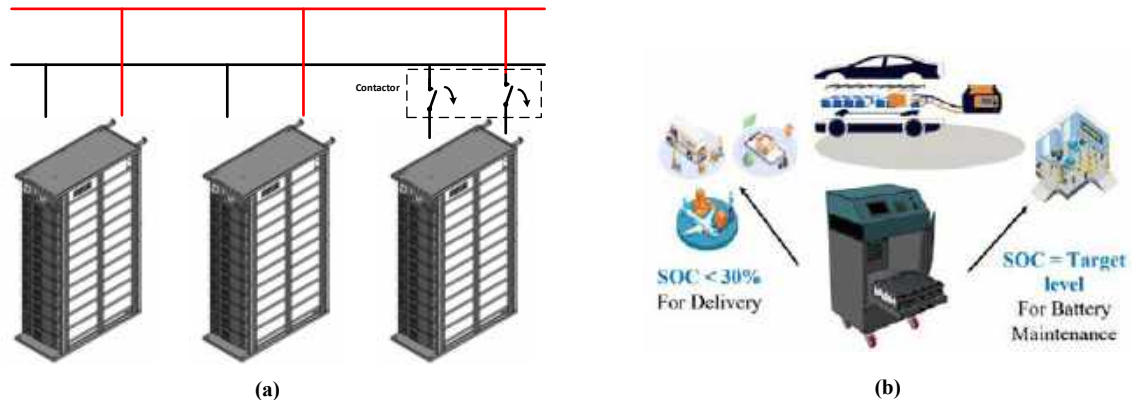


Fig. 4.2 Modular equalization in: (a) Battery energy storage system; (b) Maintenance in car repairing shop.

is guaranteed, the modular equalization is still not taken into account. On the academic side, a few research on the modular equalizer structure was introduced. The typical BMS structure of the series-connected battery modules is reported in Fig. 1.11, where a battery module is monitored by a local BMS. The data is sent to the global BMS for monitoring and control decision [75–77]. For the illustrative purposes, the conventional structural concept is presented in Fig. 4.3(a), and has adopted the converter-based equalizer. Based on the measured cell voltages from BMIC circuits, the equalization strategy for the cells is decided. In addition, another converter is used to exchange the energy of the modules via the balancing bus.

Firstly, the energy efficiency of the converter is rather low due to low handling power, although the equalization capability of the conventional structure is good. In addition, conventional structures have a bulky size and high cost.

Secondly, the equalization strategy relies on the measured voltage of the cells from BMIC, which is sensitive to noise during the equalization process. Due to the voltage dropped on the cable and connector resistance, the measured voltages of two adjacent cells are not accurate

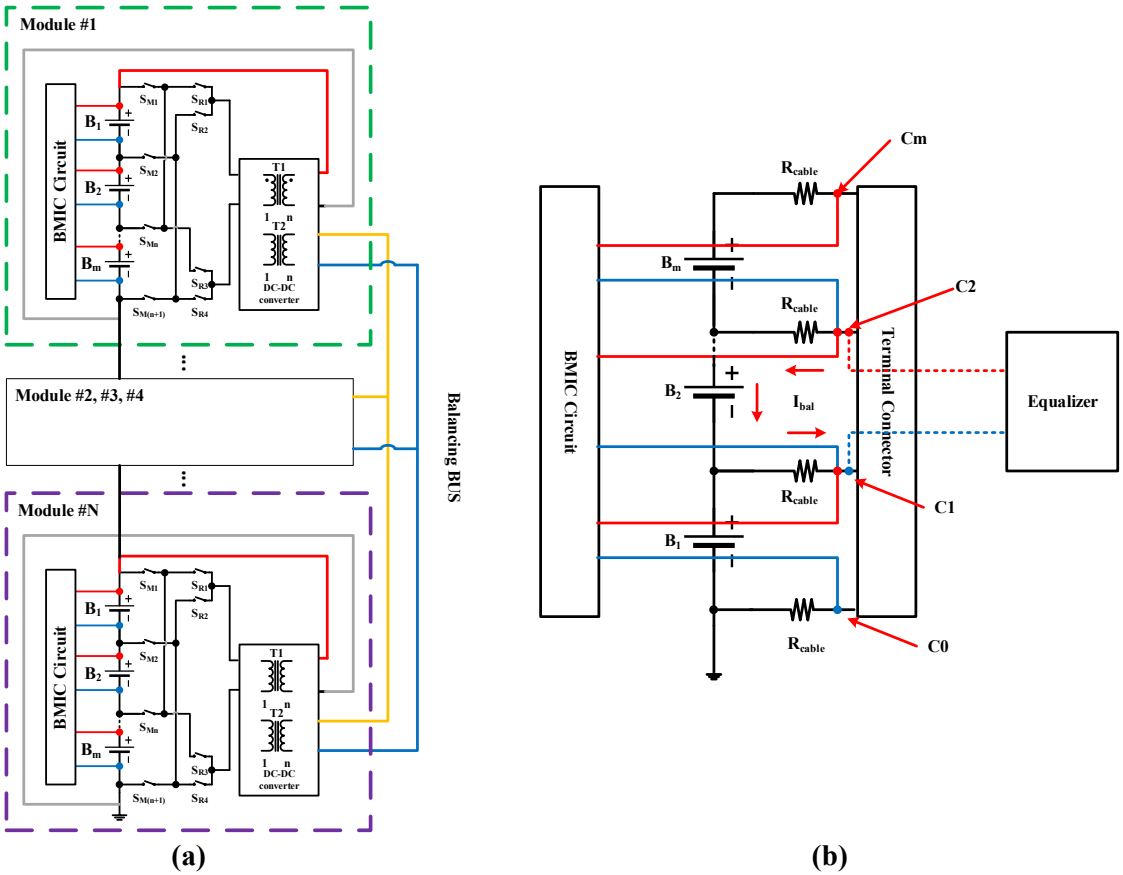
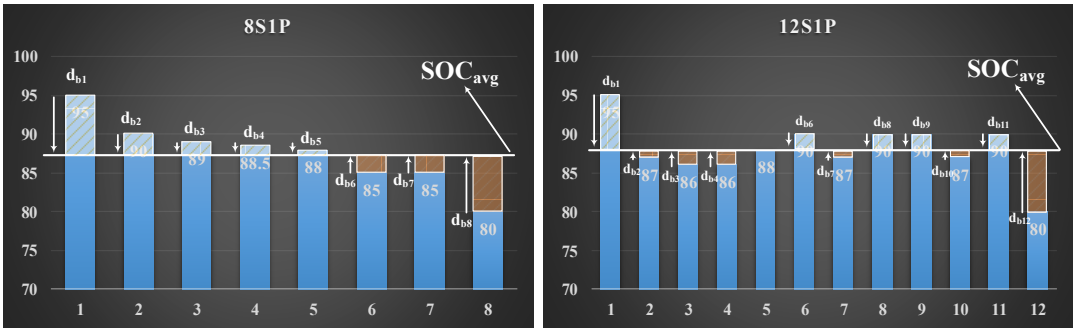


Fig. 4.3 Conventional equalizer structure for the multiple battery modules.

as in Fig. 4.3(b). If the equalization strategy is decided by the measured cell voltages, a bad decision can be made which makes the equalization process becomes ineffective.

4.1.2 Equalization Speed vs. Number of Cells

In Chapter 3, the RTSS-based and UA-model-based simulations show a homogeneous performance and equalization speed of the SMC-E even when the initial energy distribution of the cells is different. It is observed that the homogeneous speed of SMC-E is achieved only when the number of cells and the energy levels of the cells are the same. When the initial energy level of the cells in two tests are different, the equalizing time is changed as in Fig. 2.17 in Chapter 2. The difference in equalization time between the two tests is due to the



(a) (b)

Fig. 4.4 Influence of cell number to the equalization: (a) in 8S1P battery string; (b) in 12S1P battery string.

total amount of charge transferred during the equalizing process. For illustrative purposes, the equalizing process of 8S1P and 12S1P battery strings is presented in Fig. 4.4. Although the initial SOC deviation between the highest-SOC cell and the lowest-SOC cell is similar in both cases, their initial average SOC levels are different.

To explain the difference, the total changed SOC of both cases is assessed. It is assumed that all cells are equalized at the average SOC level, SOC_{avg}, and the transferred charge of each cell, d_{bk}, is calculated by

$$SOC_{avg} = \frac{1}{N}\sum_{k=1}^{N} SOC_{bk}, \tag{4.1}$$

$$d_{bk} = (SOC_{bk\_init} - SOC_{bk\_after})Q_{bk}, \tag{4.2}$$

where $(k = 1,\ 2, ...,\ N)$ and N is the total number of cells; SOC_{bk_init} and SOC_{bk_after} are the SOC level of the cell before and after the equalization process; Q_{bk} is the actual capacity of the cells. Vividly, the total transferred charge of a equalizing process is dependent on the capacity and initial energy level of the cells. Hence, the total changed SOC of the equalization

Table 4.1 TRANSFERRED CHARGE OF THE CELLS AFTER THE EQUALIZATION PROCESS

	B#1	B#2	B#3	B#4	B#5	B#6	B#7	B#8	B#9	B#10	B#11	B#12	SOC_{avg}	ΔSOC
SOC_{init}#	95	90	89	88.5	88	85	85	80	-	-	-	-	87.56	15
SOC_{final}#1	89	89	89	88	88	85.8	85.8	85.8	-	-	-	-	87.55	3.2
$d_{bk\_\#1}$ **[Ah]**	−9.6	−1.6	0	−0.8	0	1.28	1.28	9.28	-	-	-	-	-	-
SOC_{init}#2	95	87	86	86	88	90	87	90	90	87	90	80	88	15
SOC_{final}#2	88	88	88	88	88	88	88	88	88	88	88	88	88	0
$d_{bk\_\#2}$ **[Ah]**	−11.2	1.6	3.2	3.2	0	−3.2	−1.6	−3.2	−3.2	1.6	−3.2	12.8	-	-
SOC_{init}#3	95	90	87	87	87	88	88	88	90	86	87	80	87.75	15
SOC_{final}#3	87.75	87.75	87.75	87.75	87.75	87.75	87.75	87.75	87.75	87.75	87.75	87.75	87.75	0
$d_{bk\_\#3}$ **[Ah]**	−11.6	−3.6	1.2	1.2	1.2	−0.4	−0.4	−0.4	−3.6	2.8	1.2	12.4	-	-
SOC_{init}#4	95	90	85	90	86	85	89	88	89	87	85	80	87.4	15
SOC_{final}#4	87.4	87.4	87.4	87.4	87.4	87.4	87.4	87.4	87.4	87.4	87.4	87.4	87.4	0
$d_{bk\_\#4}$ **[Ah]**	−12.1	−4.1	3.9	−4.1	2.3	3.9	−2.5	−0.9	−2.5	0.7	3.9	11.9	-	-

scenario is expressed as

$$d_{total\_\#m} = \sum_{k=1}^{N} |d_{bk}|, \tag{4.3}$$

where m is the number of scenariod; $|d_{bk}|$ is the absolute value of the transferred charge. With the same design of the SMC-E, the equalization speed of the two cases must be equal. It is assumed that the cells in case #1 are equalized during t_1 and SMC-E requires t_2 to do the same task in case #2, the following relationship is obtained.

$$\frac{d_{total\_\#1}}{t_1} = \frac{d_{total\_\#2}}{t_2} \tag{4.4}$$

$$t_2 = \frac{d_{total\_\#2}}{d_{total\_\#1}} t_1. \tag{4.5}$$

Therefore, if the total changed charge of the cells and the equalization time of one scenario is known as a reference, the equalization time of the other scenarios can be predicted. To obtain the actual total change in voltage and equalizing time for the reference scenario, the RTSS-based and the UA-model based simulations can be implemented. For an instant,

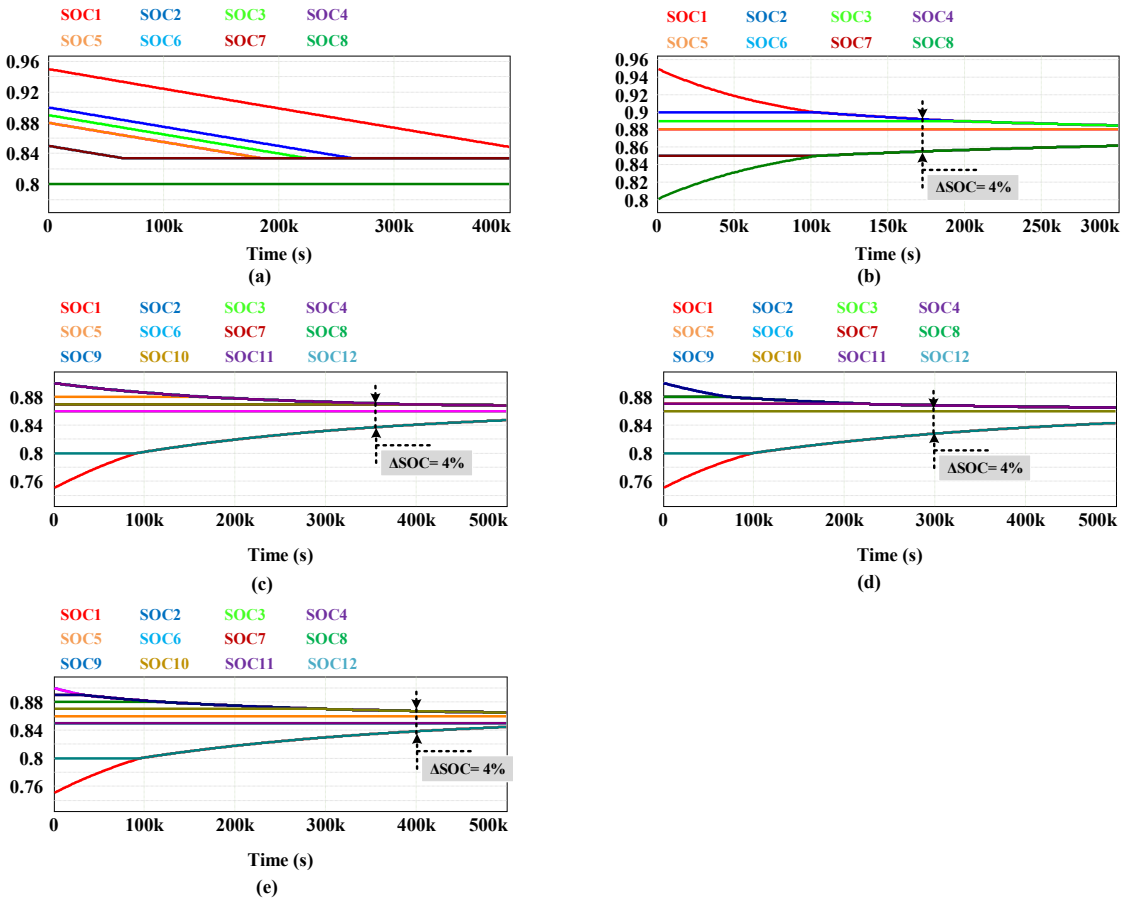


Fig. 4.5 SOC profiles of the cells during the equalization of: (a) Passive balancing method; (b) SMC-E under Scenario #1; (c) SMC-E under scenario #2; (d) SMC-E under scenario #3; (e) SMC-E under scenario #4.

the process is calculated for a 8S3P and three scenarios of 12S3P battery string (SK60 3.7V/60Ah), which have the initial SOC levels of the cells are summarized in Table 4.1. The calculation of equalization time in scenario #2, #3, #4 are follows

- Step 1: The equalization of 8S3P is implemented by UA-model based simulation. The equalization process is stopped when the cells are equalized within the average SOC level. The SOC profiles of the cells are illustrated in Fig. 4.5(b) for a visualization.

- Step 2: Based on the SOC profiles, the total transferred charge is calculated. In this case, $d_{total\_\#1}$ is $23.84Ah$. In addition, the equalization time is $48.6h$ for the reference scenario.

• Step 3: It is assumed that the cells are equalized within the average SOC level after the equalization process of scenario #2, #3, and #4. Thus, the total transferred charges of the cells are $48Ah$, $40Ah$, $52.8Ah$.

• Step 4: By using (4.5), the equalization time of the scenarios #2, #3, and #4 are $97.85h$, $81.54h$, and $107.63h$. The equalizing processes in three scenarios are verified by the UA-model based simulations to verify the calculated t_2. The SOC profiles of the cells are illustrated in Fig. 4.5(c), Fig. 4.5(d), and Fig. 4.5(e), respectively. Compared with the calculated equalization time, the mismatch between the calculated time and the actual time is small.

On the other hand, the equalization time of the SMC-E is compared to the time of the passive balancing method. Because the cells are discharged by the individual resistor, the equalization process of the cells can be simultaneously and individually executed. Thus, the equalization time of the passive method is the same in every case of cell number. In the 8S3P string, the passive method requires 111.2h to balance the cells within 4% of SOC difference. It is observed that the overall equalization speed of the SMC-E is almost similar to the passive method when the number of cells is 12. It is observed that this result is found to be correct only with a specific circuit design and test cases. Consequently, it is necessary to improve the equalizing speed of the SMC-E.

Since the equalization time of the 12S3P string in the simulation is almost similar to the calculated time, the scale-up process can be applied to the actual number of cells. It is observed that the equalizing time is longer when the number of cells increases. It is the inherent disadvantage of the SMC-E, where only two cells are equalized at a time. To overcome the disadvantage, the equalizer can be divided into multiple sub-SMC-E units

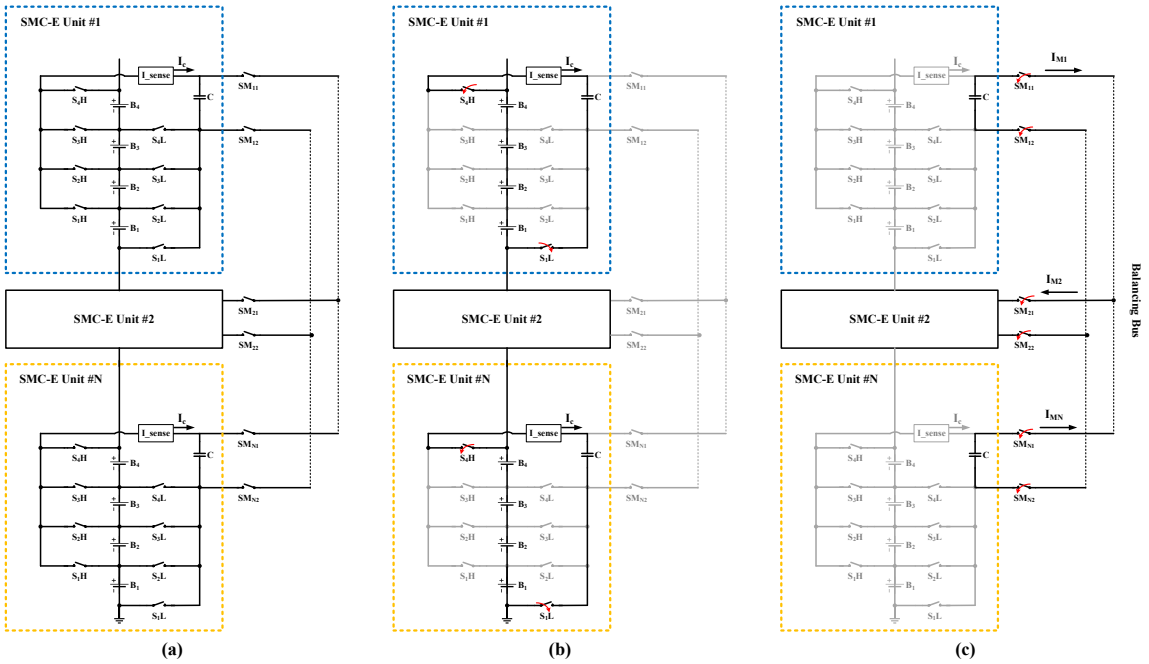


Fig. 4.6 Proposed modular equalization strategy for series-connected battery modules: (a) topology configuration; (b) Phase MA; (c) Phase MB.

and their operations are simultaneous. Thus, the overall equalization speed of the system increases. In this thesis, the series string is divided into multiple sub-modules, which are equalized by multiple SMC-E units. Since the performance of the SMC-E unit is verified for the cell level, the design of the SMC-E unit is extended for the modular equalization in Section 4.1.3. Two control strategies are proposed to equalize the energy level of the cells and modules.

4.1.3 Module Equalization Strategy for the Series-connected Modules

The topological configuration is illustrated in Fig. 4.6(a), where a SMC-E unit is implemented for every module. Furthermore, two switches SM_{k1} and SM_{k2} ($k = 1,\ 2, ...,\ N$) are added for each SMC-E unit to connect their balancing capacitors in parallel and form a balancing bus.

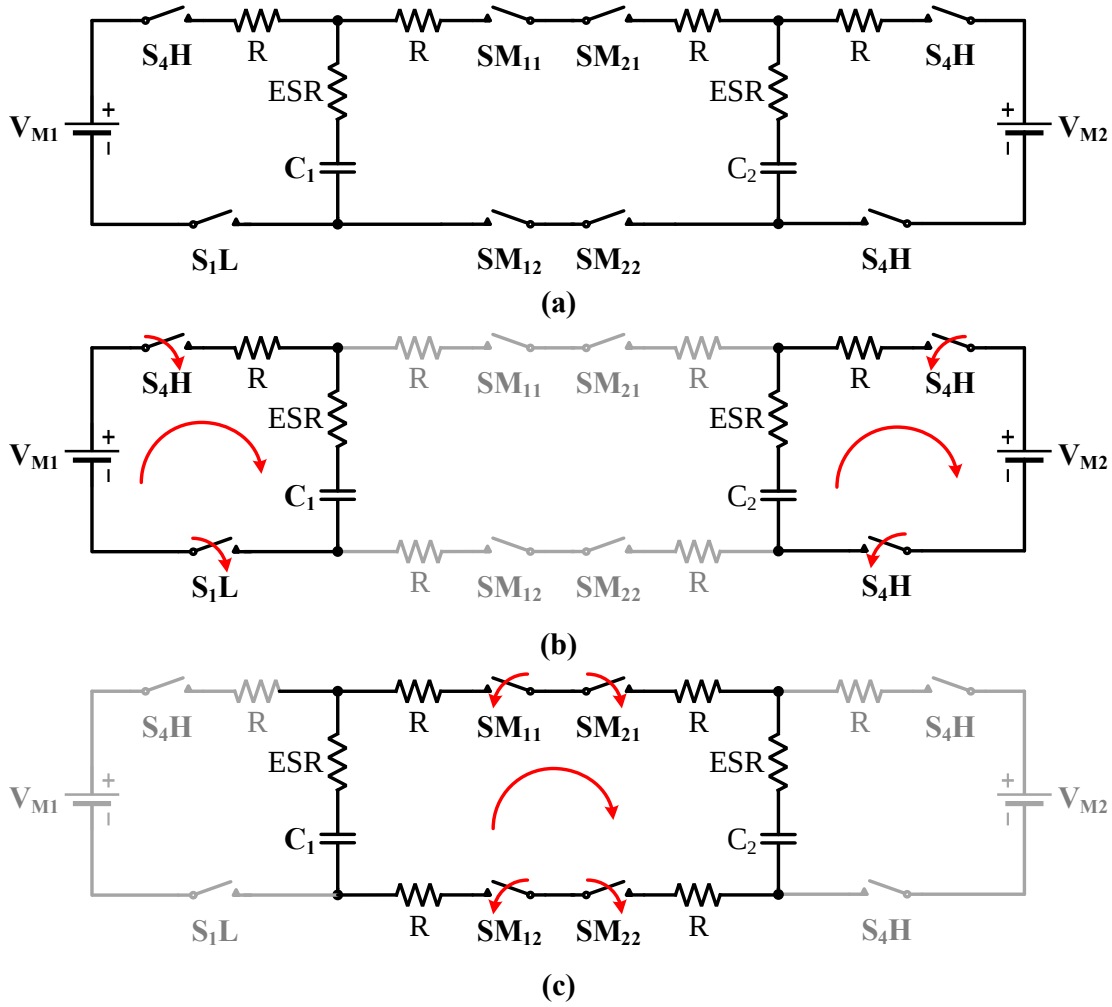


Fig. 4.7 Operating principle of the module balancing: (a) Equivalent circuit of two modules; (b) Phase MA; (c) Phase MB.

While the operation of the SMC-E unit at the cell level is similar to Chapter 2, the module balancing function can be executed either in autonomous control or governed control.

The main operating principle is presented by the equivalent circuits in Fig. 4.6(b) and (c). Similar to the operation of the cell-level equalizer, the equalizing process is divided into two phases as MA and MB. In the phase MA, the upper switch of the last cell (S_4H) and the lower switch of the first cell (S_1L) are turned on while the others are turned off as in Fig. 4.7(b). It is assumed that the voltage of module #1 is higher than that of module #2,

module #1 will charge the capacitor, C_1, by I_{M1} while capacitor, C_2, discharge to module #2 by I_{M2}. The current I_{M1} and I_{M2} are calculated by

$$I_{M1}(t) = \frac{V_{M1} - Vc(t)}{R_{loop}} exp\left(\frac{-t}{R_{loop}C_1}\right), \tag{4.6}$$

$$I_{M2}(t) = \frac{Vc(t) - V_{M2}}{R_{loop}} exp\left(\frac{-t}{R_{loop}C_2}\right), \tag{4.7}$$

where R_{loop} is the sum of the capacitor ESR, the on resistance of the switches, and the resistance of the wiring. Because four switches are always activated at the same time and the series-connected cell impedance is large, the loop resistance of the module-level equalization becomes higher than that of the cell-level equalization.

Next, all switches of the SMC-E unit are turned off and the additional switches SM_{k1} and SM_{k2} are activated to connect the balancing capacitor of the SMC-E units together in parallel. Since every parallel connection has self-balancing effect, charge will be automatically balanced between them as in Fig. 4.7(c). The voltages of the capacitors are balanced to the average voltage of all capacitors.

$$V_{M\_avg} = \sum_{i=1}^{N} \frac{1}{N} V_{Mk}, \tag{4.8}$$

where N is the number of modules and V_{Mk} is the voltage of the modules. Hence, C_1 is discharged while C_2 is charged by

$$I_{M1}(t) = \frac{V_{M1} - V_{M\_avg}}{R_{loop}} exp\left(\frac{-t}{R_{loop}C_1}\right), \tag{4.9}$$

$$I_{M2}(t) = \frac{V_{M\_avg} - V_{M2}}{R_{loop}} exp\left(\frac{-t}{R_{loop}C_2}\right), \tag{4.10}$$

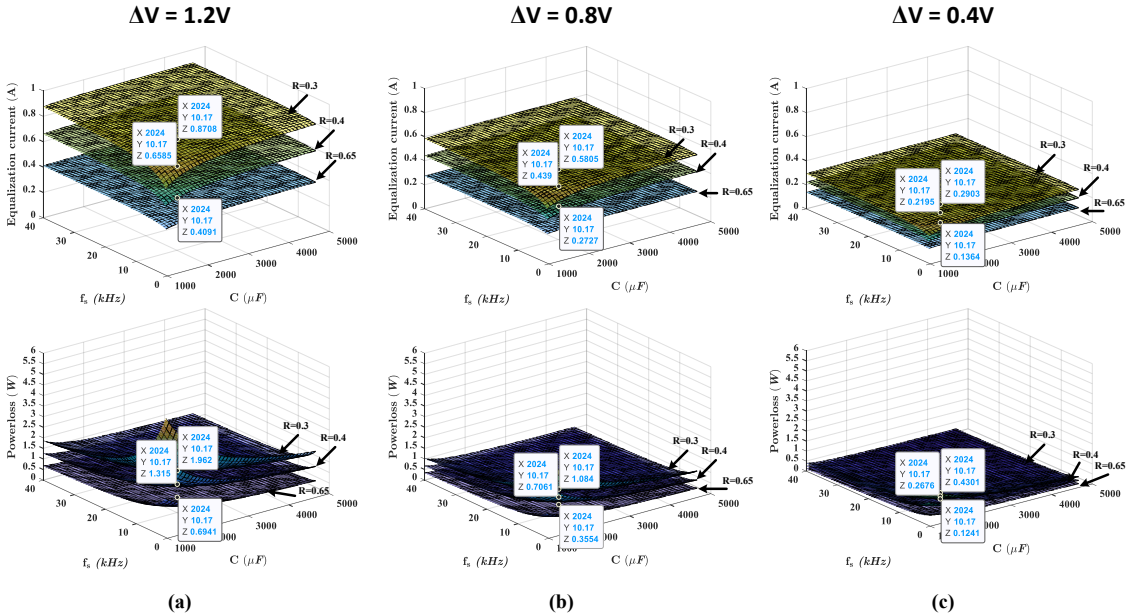


Fig. 4.8 Average current and power loss of the equalizer: (a) $\Delta V = 1.2V$; (b) $\Delta V = 0.8V$; (c) $\Delta V = 0.4V$.

Similar to Chapter 2, the operation of the switched capacitor during module equalizing process can be analyzed by its average quantity. The average equalizing current of each module are expressed as

$$I_{M1\_avg} = Cf_s(V_{M1} - V_{M\_avg})\left(1 - exp(\frac{-D}{f_s R_{loop} C_1})\right), \tag{4.11}$$

$$I_{M2\_avg} = Cf_s(V_{M\_avg} - V_{M1})\left(1 - exp(\frac{-D}{f_s R_{loop} C_2})\right) exp\left(\frac{-1}{2 f_s R_{loop} C_2}\right). \tag{4.12}$$

Although the mechanism of the modular equalization is similar at the cell-level, the voltage deviation and the internal resistance of the loop are higher than that of the cell-level. To ensure the performance of the equalizer at the module level, the average currents and power losses of the equalizers are calculated and illustrated in Fig. 4.8. By the same token in cell-level, the equalization current gradually reduces as the voltage deviation becomes smaller.

In addition, the internal resistance of the battery string also affects the equalizing speed. For example, assume that the internal resistance per battery cell is $50m\Omega$ and the total resistance of the circuit is $150m\Omega$, the total resistance of one 4S1P module becomes $300m\Omega$. Therefore, the internal resistance of the circuit must be minimized to ensure equalization speed. In addition, it is observed that the average currents and power losses of the equalizer become relatively low when the voltage deviation is small. Thus, there is a trade-off between the equalization speed and the energy loss for the equalization process.

4.1.4 Hybrid Control Algorithm Between the Cell and Module Equalization

For the modular equalization, two control strategies are proposed: a hybrid strategy and an autonomously strategy. The flowcharts are illustrated in Fig. 4.9, respectively.

Hybrid governed-autonomous strategy:

Although the equalizing processes of the cells and the modules are independent, only an equalizing pattern should be allowed at a time to prevent the short circuit between the cells. Thus, the equalization strategy for the cells and modules must be scheduled. In the hybrid strategy, the cell-level equalization inside every module should have a higher order of priority than the equalization of the modules as shown in Fig. 4.9(a). For every module, the optimal pairing algorithm is executed for the cells to achieve the fastest equalizing speed. After all modules are internally equalized, the modular equalization is triggered by the autonomous control.

During the equalization, the equalizing currents of every module are monitored. When the equalizing current of a module is lower than a threshold level, the modular equalizing process of that module will be terminated. After the equalizing process of every module is

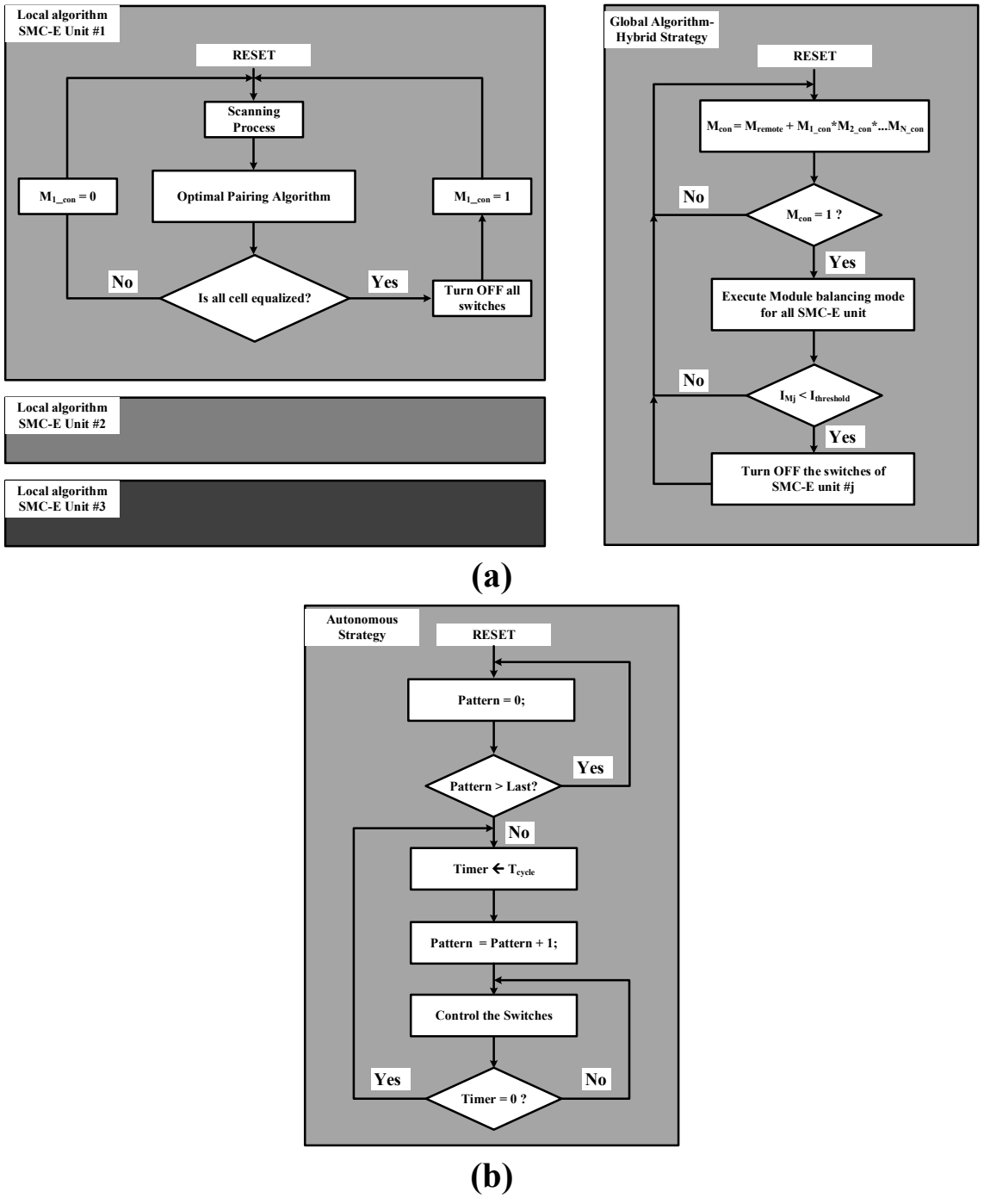


Fig. 4.9 Control flowchart for the equalization of both cell and module levels: (a) Hybrid governed-autonomously strategy; (b) Full autonomously strategy.

terminated, the inconsistency condition of the cells is periodically scanned to trigger the equalizing process for the cells and modules again.

On the other hand, because the inconsistency of the cells inside the modules is different from each others, the cell equalizing time of each module is different. Therefore, in some cases, the modular equalization would have to wait for all modules to be internally equalized and prolong the overall process. Although the hybrid strategy can guarantee the equalization capability, the governed strategy for the cells requires a high-accuracy sensing circuits, which increases the cost and volume of the system.

Autonomous strategy:

To eliminate the waiting time and the performance dependency on sensing circuits of the hybrid strategy, the autonomous strategy is proposed. With the autonomous control strategy, the cell and module equalization will be executed in turn as in Fig. 4.9(b). Each stage of operation is processed during the same duration, T_{cycle}. When the last pattern is finished, the counter is reset to repeat the autonomous equalization from the beginning.

In the autonomous strategy, the sensing circuit is disabled. Thus, the BMS cannot detect the location of the highest-voltage and lowest-voltage cells when the cell-inconsistency is arbitrary. Thus, every equalization pattern is executed in turn to transfer energy from the highest-voltage cell to the lowest-voltage cell. Thus, the equalizing pattern which balances two cells of equal voltage will product a low equalizing current. In this case, the equalization time of this step becomes ineffective. Thus, the autonomous control strategy has a lower speed than the optimal pairing algorithm for the cells.

To increase the equalizing speed, the divide and conquer sorting algorithm is adopted. As mentioned, the series cell string is divided into multiple modules, which are equalized by a SMC-E unit. Inside a module, the cells are divided into multiple groups which consist of multiple series cells. Since the number of cells can be odd or even, two dividing strategies

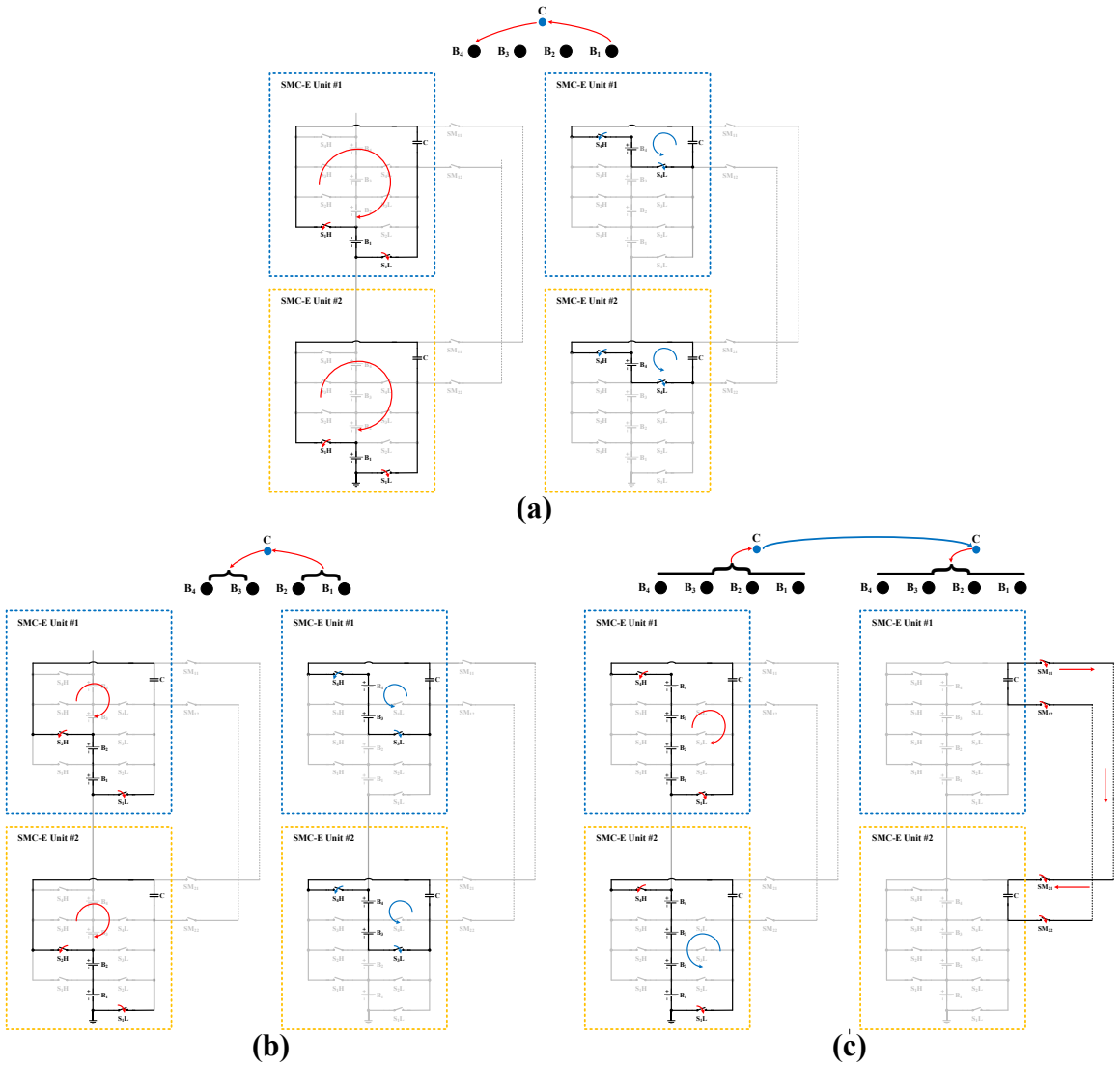


Fig. 4.10 Switching pattern of the autonomous control strategy: (a) cell-to-cell; (b) Sub-module to sub-module; (c) Module-to-module.

are illustrated in Fig. 4.11. If the number of cells is even, the module is divided by an even number such as 2, 4, etc., as in Fig. 4.11(a). In the case of an odd number of cells, there is a cell will be grouped into both sub-module as in Fig. 4.11(b). By equalizing the sub-modules together, the energy levels of multiple cells can be adjusted at the same time. Finally, the cells inside the sub-module will be equalized by a sequence of patterns, which balance every combination of two cells.

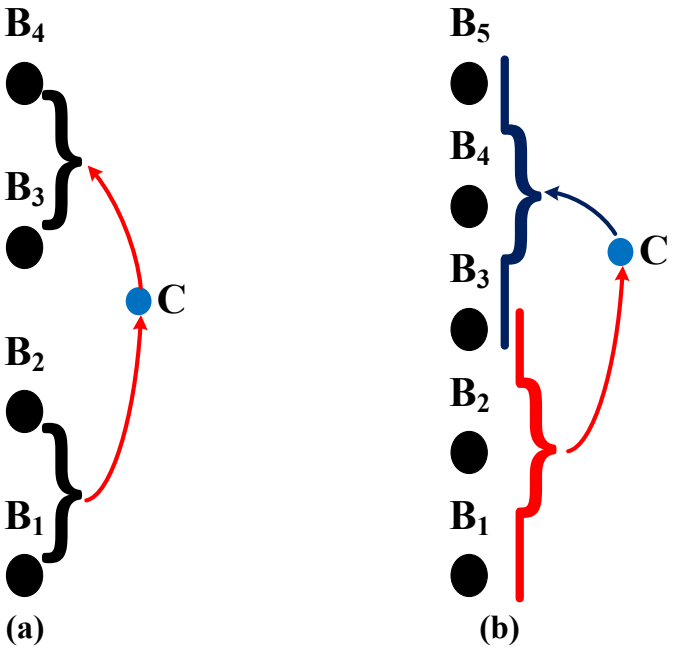


Fig. 4.11 Divide strategy in different number of cells: (a) Even dividing; (b) Odd dividing.

For illustrative purposes, a battery system consisting of two series modules is considered. The switching pattern is illustrated in Fig. 4.10. The pattern sequence starts with cell-to-cell equalization, in which every cell is paired one-by-one. The equalizing process of the cells is illustrated in Fig. 4.12(a), where the changed cell voltage levels are illustrated after every equalizing pattern. After a sequence of pattern, the energy is transferred from the highest-voltage cell to the lowest-voltage cell.

Next, the switch-matrix is controlled to balance the energy level of the two groups together as in Fig. 4.10(b) and Fig. 4.12(b). Finally, the switch-matrix pattern is changed to module-to-module equalization as in Fig. 4.10(c), when multiple modules are equalized. As a result, the energy level of the modules is gradually equalized. After the energy level of the cells inside every module is already equalized, a level III of equalization is achieved.

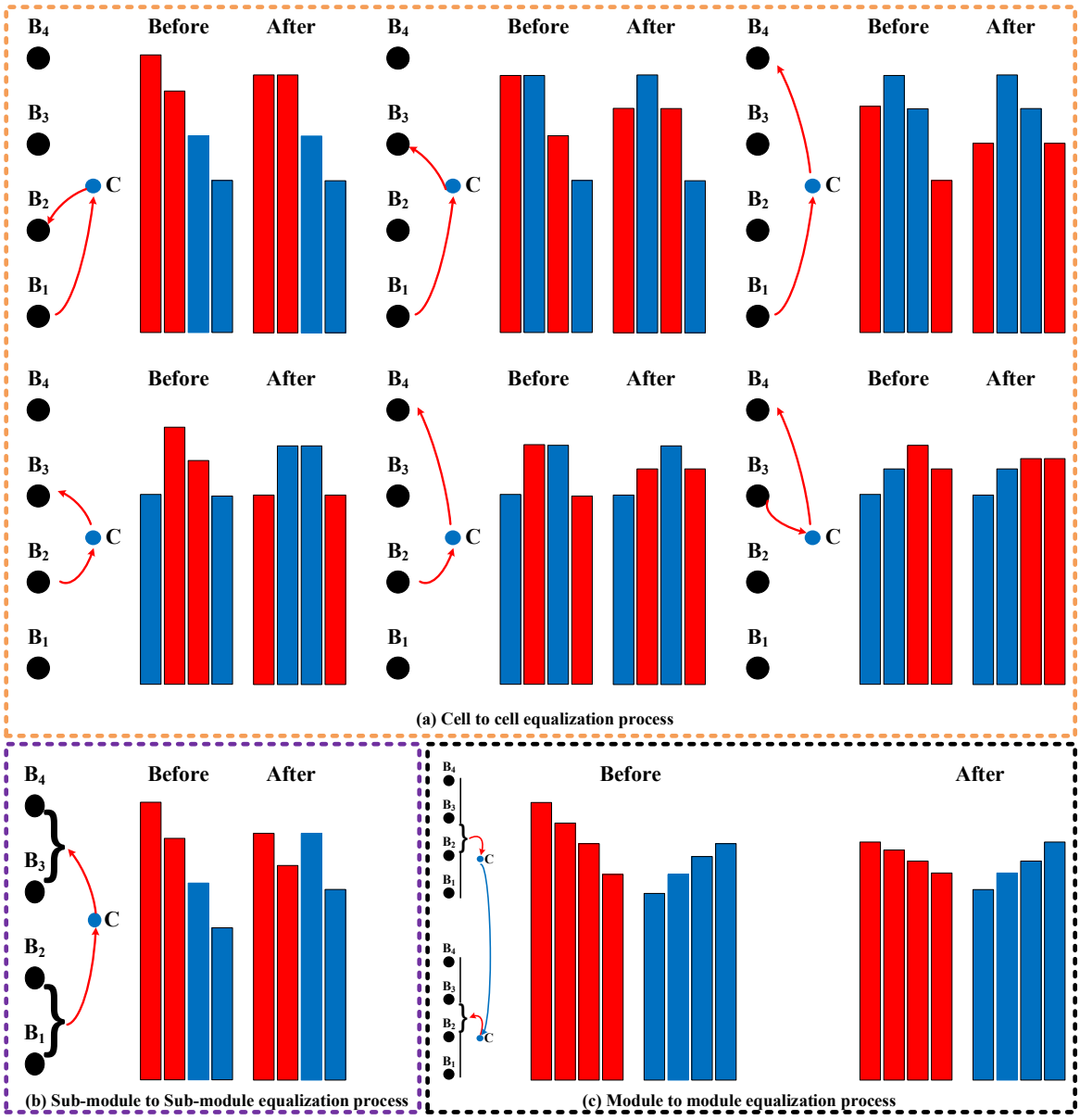


Fig. 4.12 Graphic illustration of the equalization by the autonomous control strategy: (a) cell-to-cell; (b) Sub-module to sub-module; (c) Module-to-module.

4.1.5 Design Consideration

Because the modular structure re-utilizes the hardware of the SMC-E unit, their design is almost similar. Only two switches SM_{k1} and SM_{k2} $(k = 1, 2, ..., N)$ are added to construct the module exchange bridge. On the other hand, the voltage rating of the switches $S_N H$

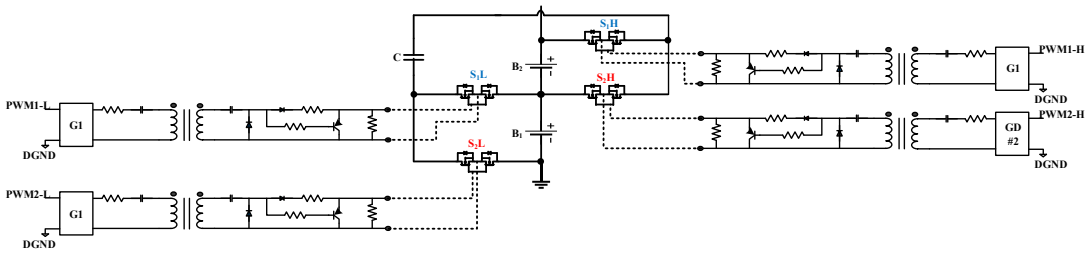


Fig. 4.13 Schematic of the gating for the modular SMC-E unit.

and S_1L, which connect the entire module to the capacitor, must be higher than the other switches. The voltage rating of the switches is calculated by

$$V_{Switch} > V_{module} + I_{bal} R_{module}, \tag{4.13}$$

where R_{module} is the total resistance of all series cells, I_{bal} is the balancing current of the modules.

On the other hand, the switches in the switch-matrix must be independently controlled for the sub-module to sub-module equalization. In this thesis, the switches S_jH and S_jL are individually controlled by the 1:1 pulse transformer circuits as in Fig. 4.13, and thus, any switching pattern can be constructed.

4.1.6 Performance Verification

To verify the performance of the modular equalization strategy for series connected modules, the proposed strategies are implemented for two series modules, which consist of 4 series-connected cells for each. In this test, the capacity is similar for 8 cells (3.6V-2.6Ah) but the initial SOC levels are set to a descending distribution order. The test setup is summarized in Table 4.2 showing a SOC deviation of 25% between the cells of each module. The average

Table 4.2 TEST SETUP ON RTSS FOR SERIES MODULAR EQUALIZATION

Parameters	Setup
C_1 & C_2	$2048\mu F$
f_sw	$10kHz$
R_{loop}	0.15Ω
Cell specs.	$3.6V - 2.6Ah$
Initial SOC level	$M_1: \ SOC_{1,2,3,\ 4} = 95,\ 85,\ 80, 70\% \ \mid \ M_2: \ SOC_{5,6,7,\ 8} = 85,\ 75,\ 70, 60\%$

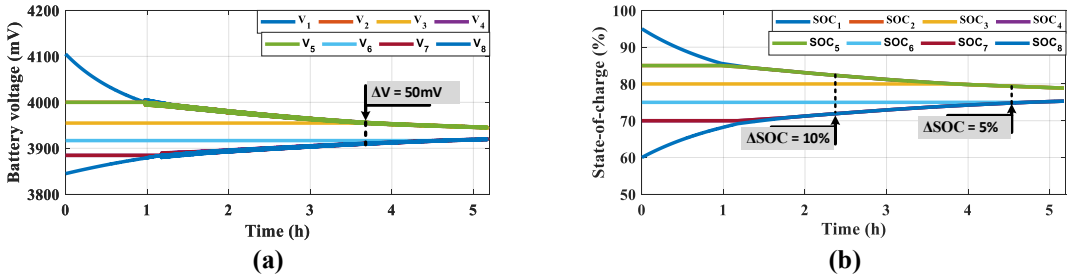


Fig. 4.14 Operating profiles of single SMC-E for 8S1P string: (a) Voltage profiles of the cells insides the modules; (b) SOC profiles of the cells.

SOC level of module #1 is set to higher than that of module #2 by 20% difference. To balance the energy of all cells, both hybrid strategy and autonomous strategy are implemented.

Hybrid Strategy

To get a reference, an 8S1P cell string is equalized by a SMC-E and the operating principle is similar to the Chapter 2. After 5.2h, the equalization is stopped to assess the equalization performance. The cell voltage and SOC level profiles are illustrated in Fig. 4.14. After the equalizing process, all cells are equalized within a voltage deviation of $30mV$ and a SOC difference of 4%. The calculated $DoSE$, $DoVE$, SR_V, and SR_S are 84%, 85.6%, 42.3 mV/h, and 4.04%/h, respectively.

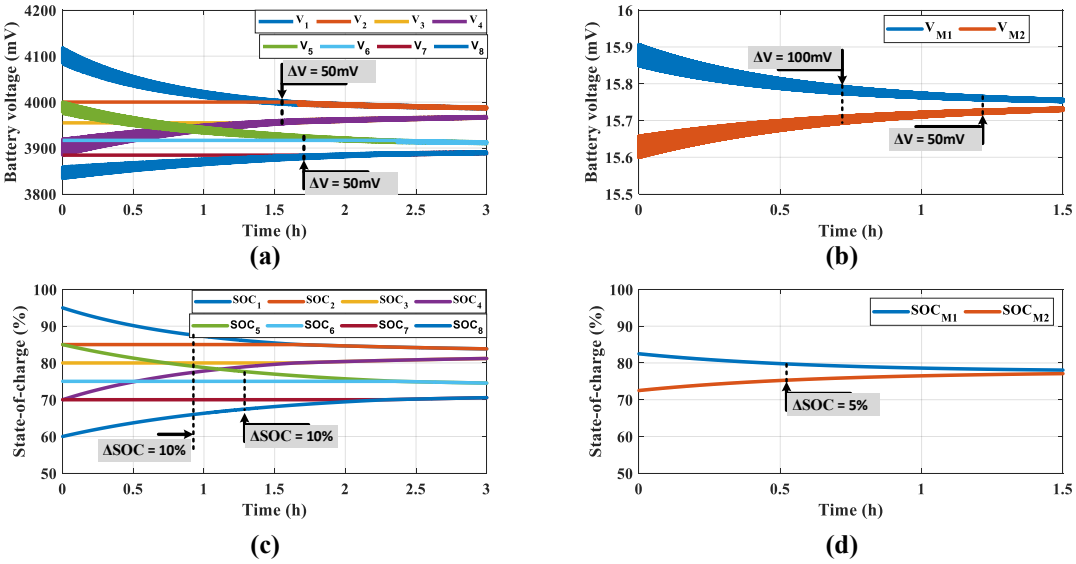


Fig. 4.15 Operation profile of the governed strategy: (a) voltage profile of the cells insides the modules; (b) voltage profile of two modules; (c) SOC profile of the cells insides the modules; (d) SOC profiles of two modules.

Furthermore, the hybrid strategy is implemented and compared with the conventional method. Because this strategy gives a higher order of priority at the cell level more than the modules equalization, the energy level of the cells inside the modules is equalized first. The cell-equalization is terminated after 3h for the performance assessment. After that, the module equalizing process is started separately. The voltage and SOC profiles of the module equalization are illustrated in Fig. 4.15, where the equalizing profiles of the cells and modules are separately plotted. In Fig. 4.15(a) and Fig. 4.15(c), the cell equalization in module #1 and module #2 are simultaneously executed. It is observed that the cells of the module #1 are equalized within a voltage deviation of $20mV$ and a SOC difference of 2.4%, respectively. The calculated DoSE and DoVE are observed by 90.4% and 90%, respectively. In addition, the cells inside module #2 are equalized within a voltage deviation of $25mV$ and a SOC deviation of 4%, respectively. It means that equalization level I is achieved for

both modules. Compared with the conventional method in Fig. 4.14, the hybrid strategy has a higher equalization capability.

In view of equalizing speed, the extended SMC-E only requires about $1.5h$ to equalize the cell voltages within a voltage deviation of $50mV$ and $3h$ for a voltage deviation of $20mV$. The relative slew rate of voltage equalization at $1.5h$ and $3h$ are $100mV/h$ and $60mV/h$, respectively. In this test, the initial energy distribution and the energy deviation of the cell in module #1 and module #2 are almost similar. Therefore, the difference of cell equalizing times between both modules are trivial. Assuming that the energy deviation in module #1 is higher than module #2, the SMC-E unit #2 finishes the cell equalization process first and the algorithm wait until the cell equalization in module #1 is completed.

Since the cell equalization in every module is achieved, the module equalization process is triggered at time 0. The voltage and SOC profiles in Fig. 4.15(b) and Fig. 4.15(d) show that the modules are equalized within a voltage deviation of $20mV$ and a SOC difference of 1% after $1.5h$ of the equalizing process. It means that the modular equalizing strategy achieves equalization level III. After the equalization, the voltage and SOC levels of all cells are equalized within a voltage deviation of $25mV$ and a SOC difference of 3%. In the test, the initial energy levels of the cells in module #1 and module #2 are set to a predefined level, which has the same initial voltage and SOC deviations. The slew rate of the voltage and SOC equalization is calculated for the whole process to compare with the conventional method. The proposed method requires only 4.5h to finish the cell and module equalization. The calculated SR_V and SR_S are 50 mV/h and $4.9\%/h$. Compared to the conventional method, modular equalization has a higher speed.

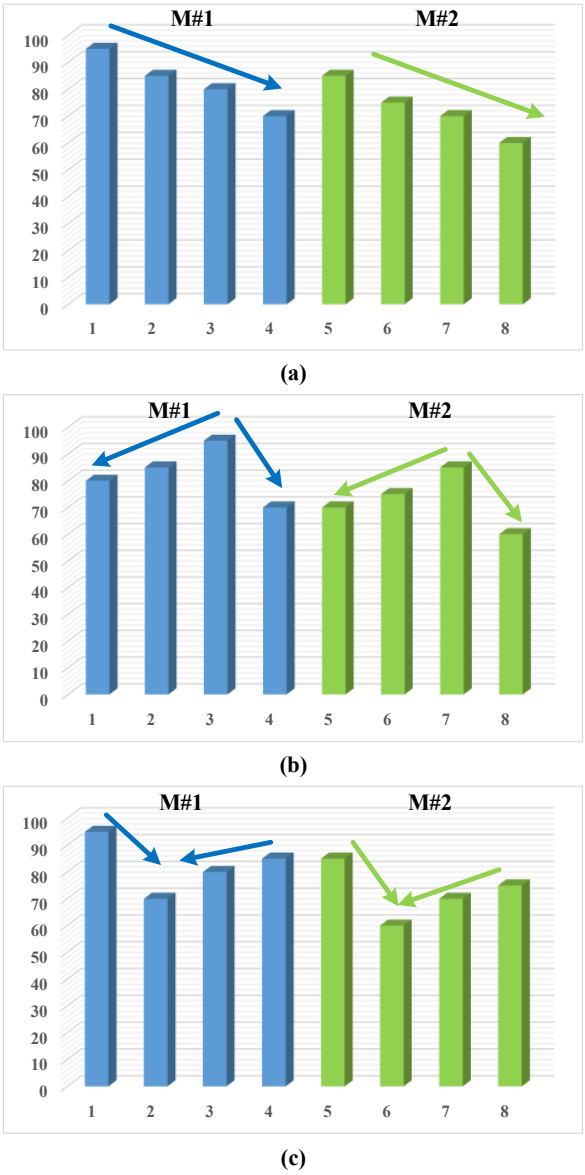


Fig. 4.16 Initial SOC distribution of the cells (Module #1- C#1, C#2, C#3, C#4; Module #2- C#5, C#6, C#7, C#8): (a) Descending distribution; (b) Convex distribution; (c) Concave distribution.

Autonomous Strategy

To assess the impact of the initial energy distribution on the performance of the autonomous strategy, the module equalizer is tested under three different scenarios as in Fig. 4.16. While the descending distribution in Fig. 4.16(a) is similar to the condition of hybrid strategy, the

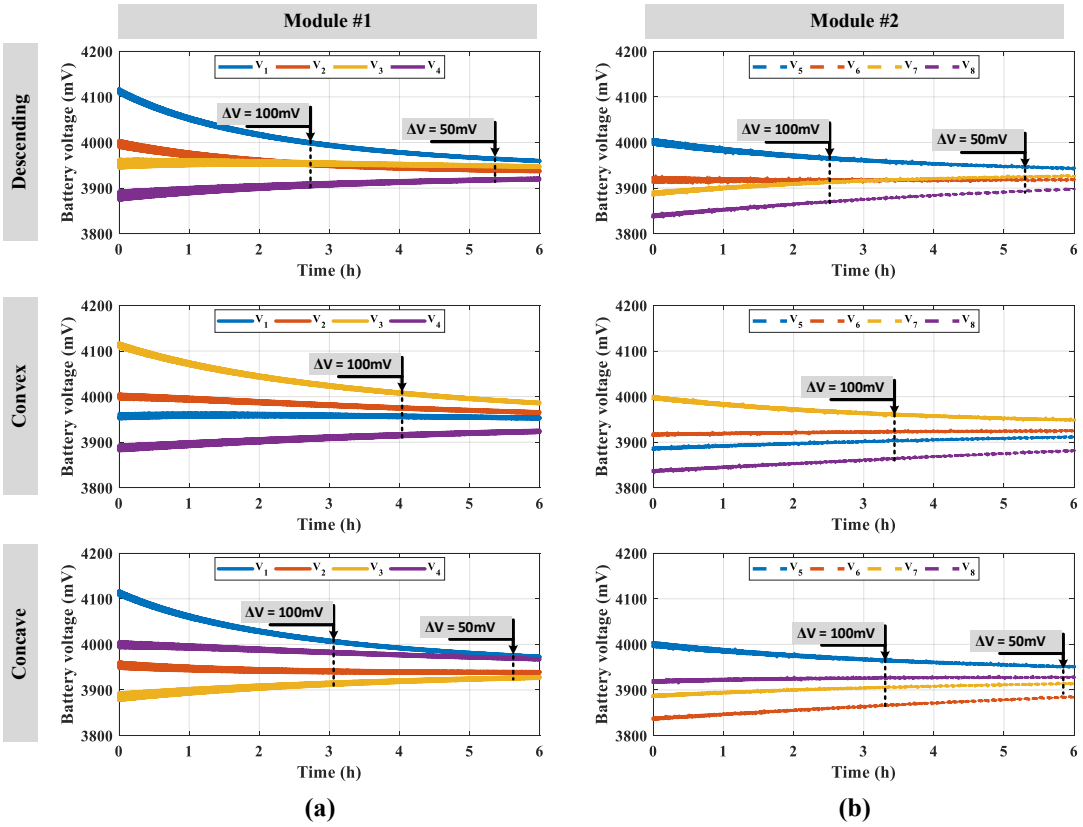


Fig. 4.17 Voltage profile of the cells during the autonomous equalization under three test scenarios: (a) Inside module #1; (b) Inside module #2.

convex and concave distributions in Fig. 4.16(b) and Fig. 4.16(c) locate the highest energy cell at the middle or two ends of the string.

The voltage and SOC profiles of every cell during the autonomous equalization are illustrated in Fig. 4.17 and Fig. 4.18, respectively. Vividly, the equalization level I can be achieved in descending and concave distribution cases after 6h. In convex cases, the equalizing speed of the autonomous strategy is slower than the others. Regardless, the equalization level I can be achieved if the process is continuously executed. Since the impact of initial energy distribution on the equalizing speed of the autonomous strategy is significant, the autonomous strategy has a slower equalizing speed than that of the hybrid strategy. It requires 5.5h to equalize the cells within a voltage deviation of $40mV$ and a SOC difference of

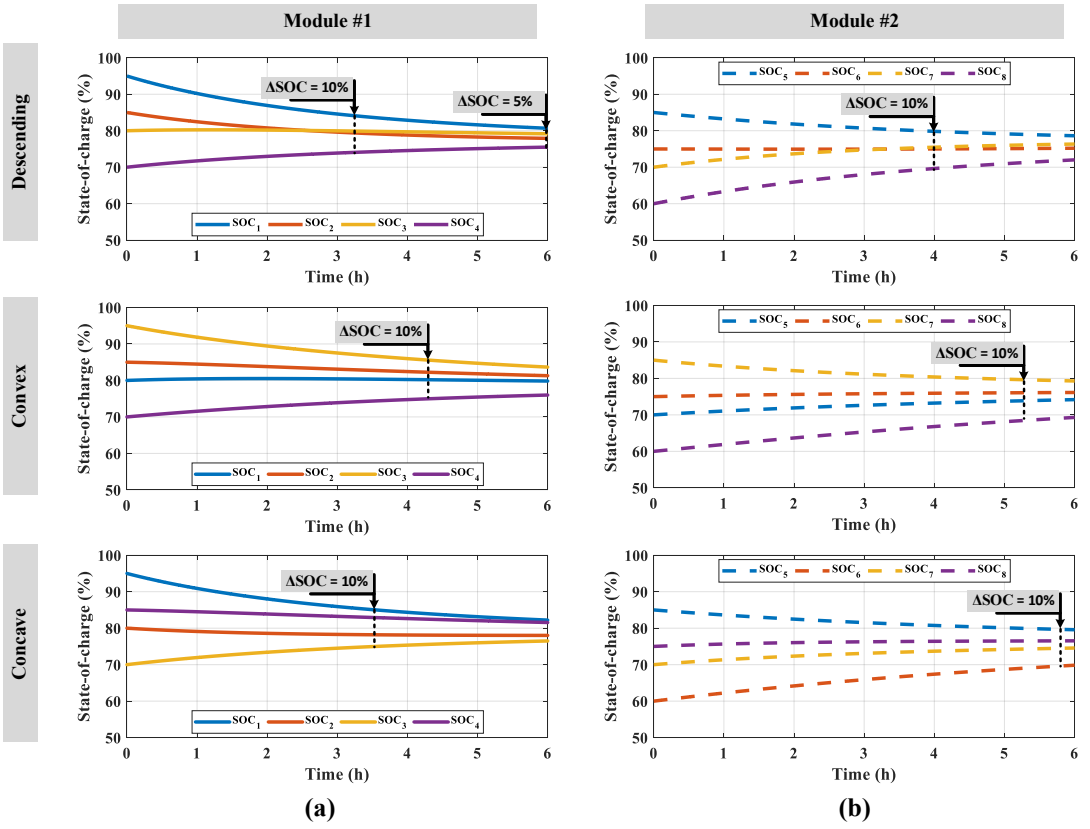


Fig. 4.18 SOC profile of the cells during the autonomous equalization under three test scenarios: (a) Inside module #1; (b) Inside module #2.

4%, while the hybrid hybrid strategy only needs 4.5h. The SR_V and SR_S of the autonomous strategy are 38.2 mV/h and 3.82 $\%/h$

To assess the modules equalization, the voltage and SOC profiles of all cells and the module-voltages profile are illustrated in Fig. 4.19. According to the results, the autonomous strategy only achieves the equalization of level I, level II, and level III in the descending distribution case. The equalization speed is slower than that in the other cases.

On the other hand, the current profile of one equalization cycle is shown in Fig. 4.20, where the equalizing patterns are step-by-step executed. When the modular equalization pattern is finished, the pattern sequence is reset from the beginning. In module #2, the

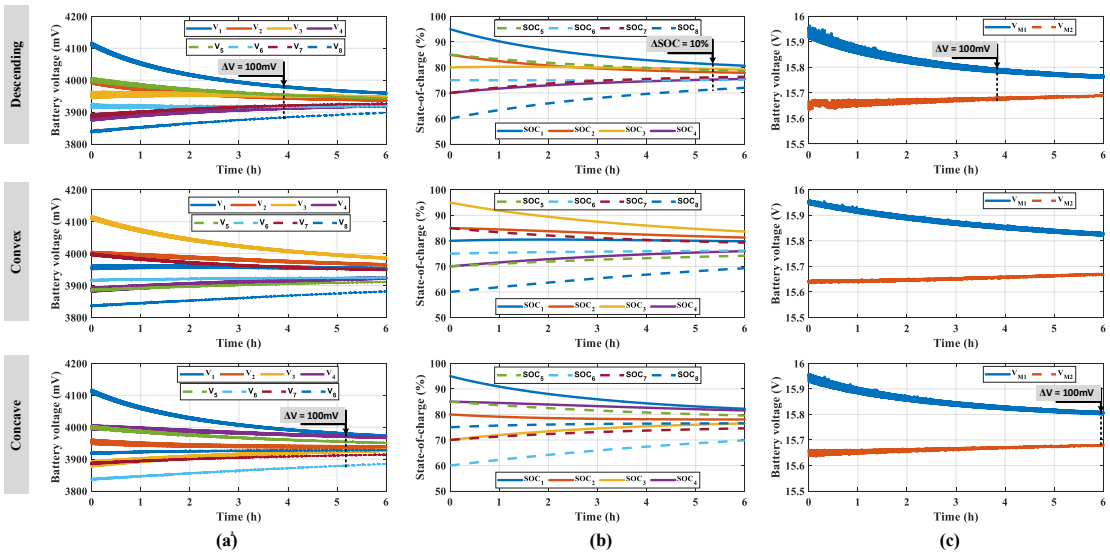


Fig. 4.19 Operation profiles during the autonomous equalization under three test scenarios: (a) Voltage profile of all cells; (b) SOC profile of all cells; (b) SOC profile of all cells; (c) Voltage profile of modules.

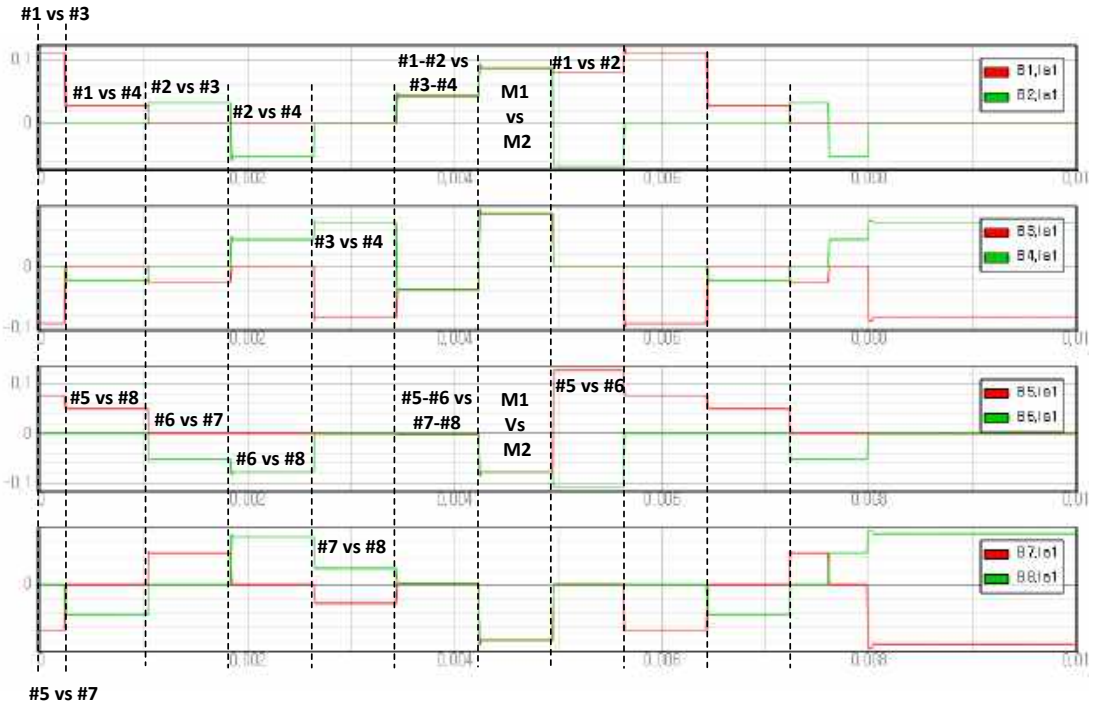


Fig. 4.20 Current profiles of one equalization cycle by autonomous strategy

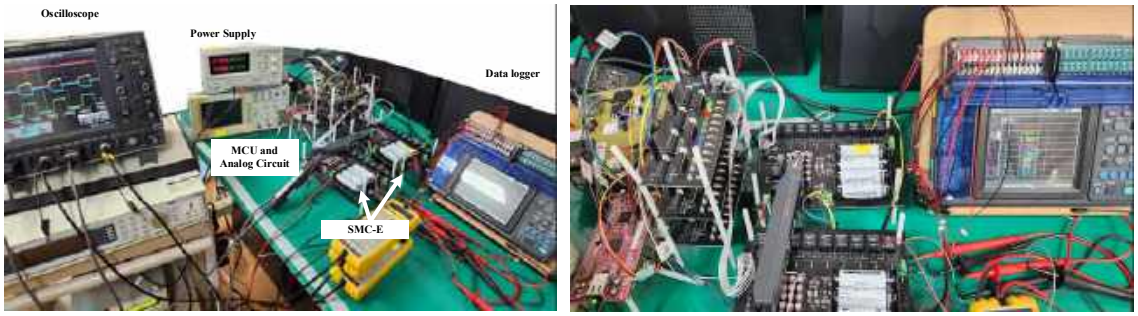


Fig. 4.21 Experimental setup of the SMC-E for modular equalizing strategy

Fig. 4.22 Hardware design of the SMC-E in every experiments

equalizing current is zero since the voltage of group #1 (cell #5 + cell #6) and group #2 (cell #7 + cell #8) are almost equalized.

To further verify the performance of the modular equalizing strategy for the series-connected modules, a prototype is made for two SMC-E modules. The experimental setup is shown in Fig. 4.21, where the operating waveform is obtained by the Lecroy oscilloscope and the cell voltages are recorded by a data logger (Hioki LR8402-20) and are plotted by Matlab software. The design of the SMC-E are summarized in Fig. 4.22, where 20 pcs of electrolytic capacitors 100 μF are connected in parallel to form a unit of equalizing capacitor. The

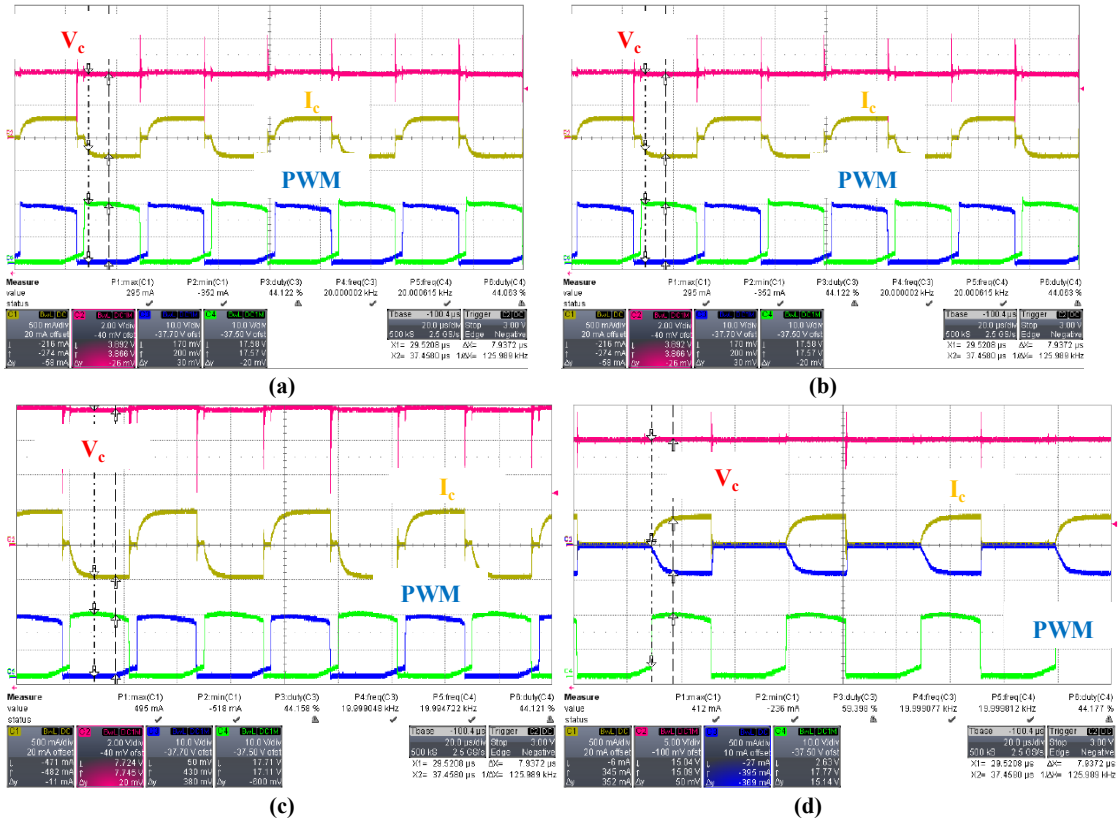


Fig. 4.23 Operating waveform of the SMC-E: (a) Cell equalization at $\Delta V = 250\ mV$; (b) Cell equalization at $\Delta V = 100\ mV$; (c) Sub-modules equalization; (a) Module equalization.

measured capacitance of the equalizing capacitor unit is similar to the calculation in Chapter 2. In all tests, the ICR18650-30A cells are docked on the battery holder of the SMC-E board.

The operating waveform of the extended SMC-E for the series module equalization are illustrated in Fig. 4.23. While Fig. 4.23(a) and (b) show a homogeneous waveform with the waveform in Chapter 2, the equalizing waveform in Fig. 4.23(c) and (d) confirm the operation of the SMC-E in the module level. In the module equalization, the voltage balancing between two capacitors occurs in a very fast way. Therefore, only the equalizing current of the battery modules can be observed.

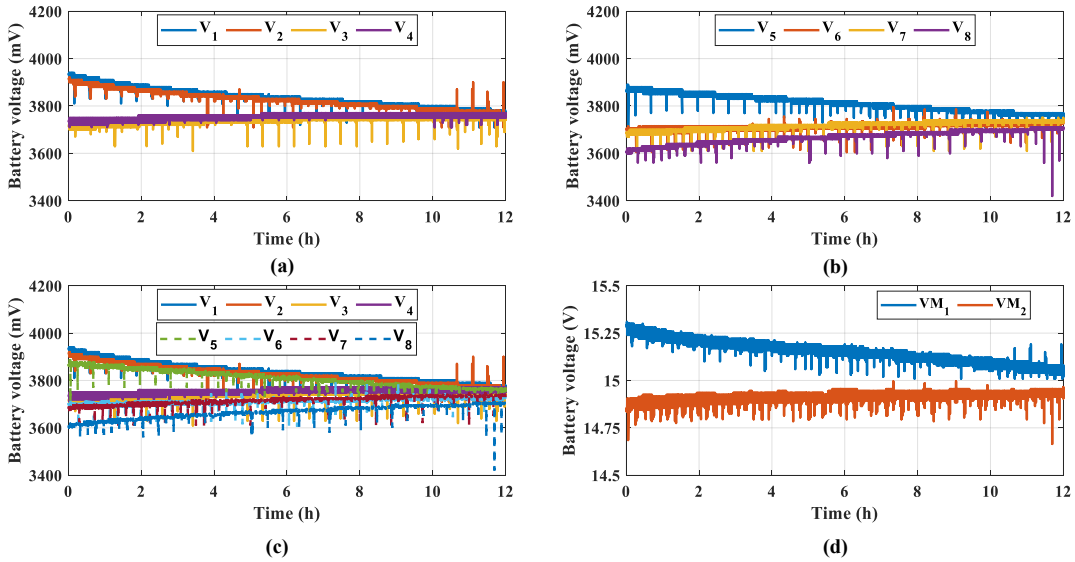


Fig. 4.24 Voltage profile during the equalizing process: (a) versus cell voltages inside module #1; (b) versus cell voltages inside module #2; (c) versus all cells; (d) module #1 versus module #2;

Furthermore, the recorded voltage profiles during the equalizing process are illustrated in Fig. 4.24. Vividly, the cells in both module #1 and module #2 are equalized within a voltage deviation of $30mV$. The equalization level III is achieved as shown in Fig. 4.24(c), where the cells are equalized within a voltage deviation of $50mV$. Considering the initial voltage deviation of $340mV$, approximately DoVE of 86% is achieved. Although the equalizing time is quite long, the equalization can be executed without any guidance of the measuring circuit. Therefore, the complexity of the control circuit can be significantly reduced.

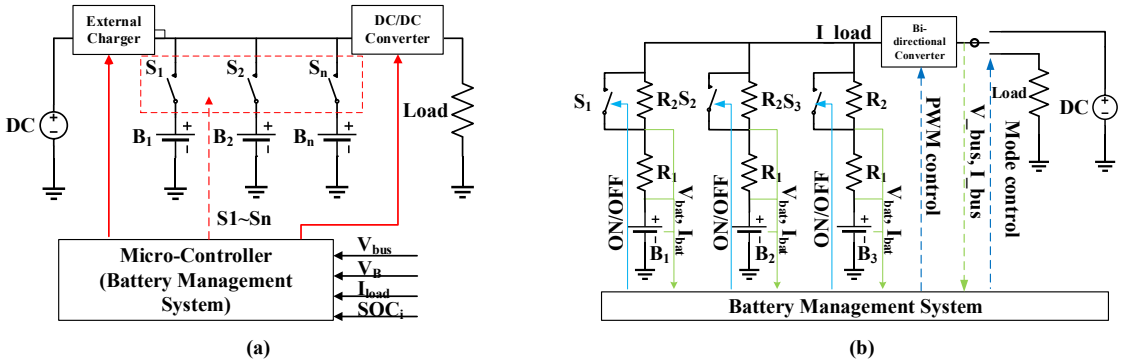


Fig. 4.25 Conventional equalization circuits of the parallel connected battery modules: (a) Relay-based scheduling method; (b) dynamic resistance equalization.

4.2 Extension of SMC-E for Parallel-connected Modules

Similar to the series connected modules cases, the same design of the SMC-E unit is adopted for the parallel connected modules. A novel strategy is developed for the energy exchanged in IDLE mode, and power distribution in non-IDLE modes including charging and discharging processes.

4.2.1 Conventional Structure

Sometimes, the battery modules are individually connected to the DC bus by a relay or contactor [94, 95]. Based on the measured voltage of the modules, the relay or contactor is switched to balance the energy level of the modules as in Fig. 4.25(a). This method can individually control the operation of the modules and can isolate the unhealthy module from the DC bus. However, an inrush current flows when the battery module is connected to the DC bus by the relay or contactor. The current profile in Fig. 4.26 shows the self-balancing effect, when four modules with different voltage levels are suddenly connected in parallel. The high-voltage modules are discharged by a high current and the lower energy module is charged by a high current. Such a high initial current can damage to the battery module.

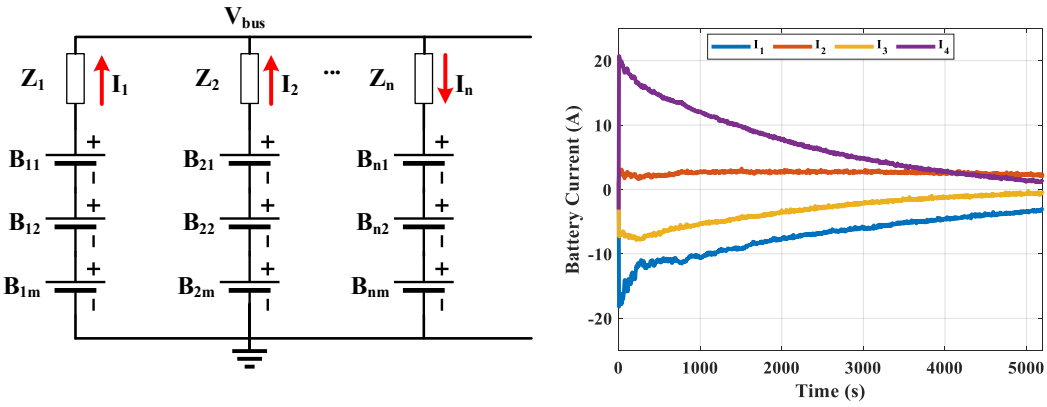


Fig. 4.26 Self balancing effect in the parallel connected battery module when they are connected together at t=0

To suppress the inrush current and make the branch currents even, the dynamic resistance equalizer in Fig. 4.25(b) is introduced [25]. Technically, the switch modulates the series resistance which can regulate the branch currents. When the energy level of the modules is equalized, the switch is closed to minimize the series resistance. This method is simple, but shows good performance. However, high energy loss in the resistors is a critical disadvantage of the dynamic resistance equalizer.

In conclusion, a high-efficiency equalization method is required for the parallel-connected battery module. On the other hand, the uneven current distribution between the branches under a non-idle process should be resolved.

4.2.2 Proposed Equalization Strategy for Parallel-connected Battery Modules

The equalization of the parallel modules can be achieved through two mechanisms: energy exchange in IDLE mode and current distribution in non-IDLE mode. According to the operating mode, the corresponding control strategy is activated.

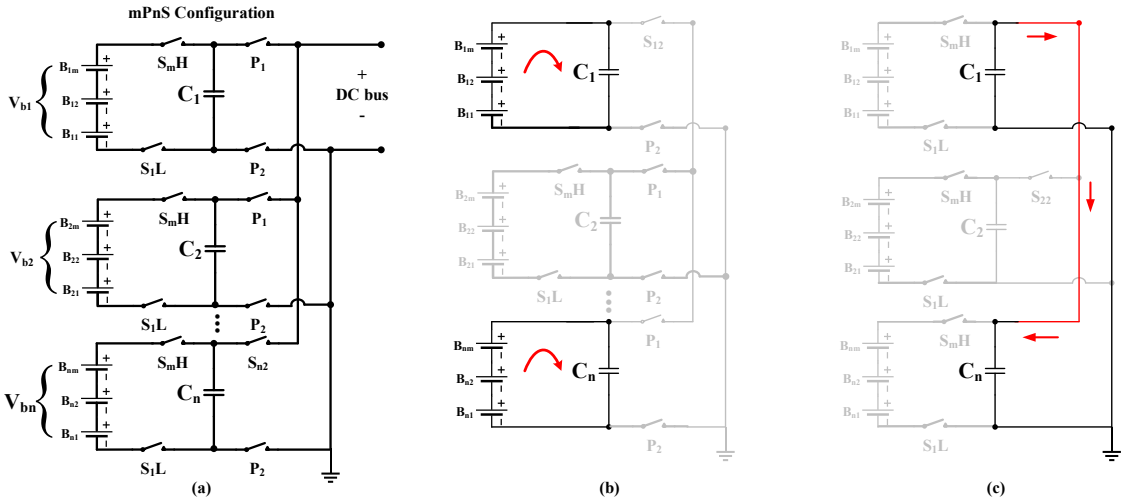


Fig. 4.27 Modular strategy for parallel connected battery module: (a) Topology configuration; (b) Operation principle - Phase A; (c) Operation principle - Phase B.

Energy Exchange Strategy for IDLE mode

The topological configuration for the parallel-connected battery modules is similar to the design of the series-connected battery modules. In addition, the battery modules are separated from each other by the switches as in Fig. 4.27(a). In the IDLE mode, where the battery system has no charge or discharge current from the DC bus, the energy exchange mechanism is illustrated in Fig. 4.27(b) and Fig. 4.27(c), where the equalizing process is also divided into phase A and phase B. The equalizing strategy for the series-connected modules can be directly adopted for the parallel connection as well.

Current Distribution strategy for non-IDLE mode

In the parallel connection, the load currents are distributed between the branches. If the module is modeled as the voltage sources and the internal impedance as in Fig. 4.28(a), the

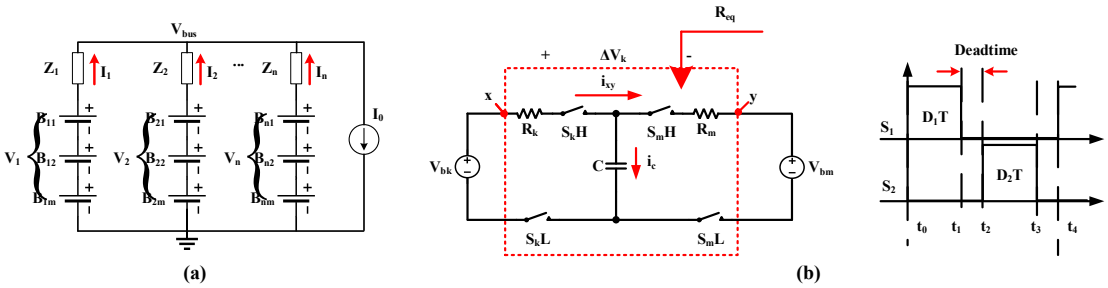


Fig. 4.28 Operation of the parallel-connected battery modules: (a) Parallel modules in discharge process; (b) Equivalent circuit of the switched capacitor equalizer.

current in each branch can be solved by the equation

$$\begin{aligned} Z_1 I_1 - Z_2 I_2 &= V_1 - V_2 \\ Z_1 I_1 - Z_3 I_3 &= V_1 - V_3 \\ &\ldots \\ Z_1 I_1 - Z_n I_n &= V_1 - V_n \\ I_1 + I_2 + I_3 + \ldots + I_n &= I_0, \end{aligned} \tag{4.14}$$

where V_1, V_2,..., V_n are the open-circuit-voltage of the battery modules; Z_1, Z_2,..., Z_n are the internal impedance of the modules; I_1, I_2,..., I_n are the operation currents of the branches. Vividly, the voltage and impedance of each battery module have a strong impact on the current distribution of the branches. If the modules with different voltage levels are directly connected, the uneven current distribution of the branches can lead some modules to the overload condition. Therefore, maintaining the uneven current distribution between the branches is required. If the branch current can be regulated by changing the branch impedance, it helps to control the current within a safety level.

The operation of the proposed topology can be explained by the equivalent circuit in Fig. 4.28(b). In phase A (t_0 to t_1), the capacitor is charged by the source V_{bk}, and the charge increment in the capacitor and the capacitor voltage difference are calculated by

$$Q_{inc} = \int_{t_0}^{t_1} i_k(t)dt = (V_{bk} - v_c(t_0))\, C \left(1 - e^{\frac{-D_1 T}{\tau_k}}\right), \tag{4.15}$$

and

$$v_c(t_1) - v_c(t_0) = \frac{Q_{in}}{C} = (V_{bk} - v_c(t_0)) \left(1 - e^{\frac{-D_1 T}{\tau_k}}\right), \tag{4.16}$$

where D_1 is the duty cycle ratio and T is the switching period. The voltage of the capacitor is constant during the dead time (t_1 to t_2) since all switches are turned off.

In phase B, the capacitor is docked to the voltage source V_{bm}, and energy is released from the capacitor to V_{bm}. Thus, the charge decrement and the capacitor voltage difference are calculated by

$$Q_{dec} = \int_{t_2}^{t_3} i_m(t)dt = (v_c(t_2) - V_{bm}) C \left(1 - e^{\frac{-D_2 T}{\tau_m}}\right) e^{\frac{-T}{2\tau_m}}, \tag{4.17}$$

and

$$v_c(t_2) - v_c(t_3) = \frac{Q_{out}}{C} = (v_c(t_2) - V_{bm}) \left(1 - e^{\frac{-D_2 T}{\tau_m}}\right) e^{\frac{-T}{2\tau_m}}. \tag{4.18}$$

In the quasi-steady state condition, $Q_{inc} = Q_{dec}$, and thus, the average balancing current is expressed as

$$\begin{aligned} I_c &= Q_{inc} f_s = Q_{dec} f_s \\ &= (V_{bk} - v_c(t_0))\, C f_s \left(1 - e^{\frac{-D_1}{f_s \tau_k}}\right) \\ &= (v_c(t_2) - V_{bm})\, C f_s \left(1 - e^{\frac{-2D_2}{f_s \tau_m}}\right) e^{\frac{-1}{2 f_s \tau_m}}, \end{aligned} \tag{4.19}$$

where f_s is the switching frequency of the equalizer. On the other hand, the voltage difference between the capacitor and the voltage source during two phases is described by

$$\Delta V_k = V_{bk} - v_c(t_0) = \frac{I_c}{f_s C} \frac{1}{1 - e^{\frac{-D_1}{f_s \tau_k}}}, \tag{4.20}$$

and

$$\Delta V_m = v_c(t_2) - V_{bm} = \frac{I_c}{f_s C} \frac{e^{\frac{1}{2 f_s \tau_m}}}{1 - e^{\frac{-2D_2}{f_s \tau_m}}}. \tag{4.21}$$

Thus, energy loss for each voltage source is calculated by

$$E_k = \frac{I_c^2}{2 f_s^2 C} \frac{1 + e^{\frac{-D_1}{f_s \tau_k}}}{1 - e^{\frac{-D_1}{f_s \tau_k}}}, \tag{4.22}$$

$$E_m = \frac{I_c^2}{2 f_s^2 C} \frac{1 + e^{\frac{-D_2}{f_s \tau_m}}}{1 - e^{\frac{-D_2}{f_s \tau_m}}}. \tag{4.23}$$

The power loss can be calculated by multiplying the energy loss with the switching frequency as (4.24). If the switched capacitor equalizer is represdented by an equivalent resistor, R_{eq}, which is seen from the $x - y$ terminal in Fig. 4.28(b), the power loss of the

equalizer can be approximately calculated by (4.25)

$$\begin{aligned} P_{loss} &= (E_k + E_m) f_s \\ &= \frac{I_c^2}{f_s C} \frac{e^{\frac{D_1}{f_s \tau_k}} e^{\frac{D_2}{f_s \tau_m}} - 1}{\left(e^{\frac{D_1}{f_s \tau_k}} - 1\right)\left(e^{\frac{D_2}{f_s \tau_m}} - 1\right)}, \end{aligned} \tag{4.24}$$

$$P_{loss} = I_c^2 R_{eq}. \tag{4.25}$$

By comparing (4.24) and (4.25), the equivalent resistance can be obtained.

$$R_{eq} = \frac{1}{f_s C} \frac{e^{\frac{D_1}{f_s \tau_k}} e^{\frac{D_2}{f_s \tau_m}} - 1}{\left(e^{\frac{D_1}{f_s \tau_k}} - 1\right)\left(e^{\frac{D_2}{f_s \tau_m}} - 1\right)}. \tag{4.26}$$

It is observed that the equivalent resistance, R_{eq}, is a function of the duty ratio, the balancing capacitance, and the switching frequency. Since the balancing capacitance is fixed by the original design, the R_{eq} can be adjusted by changing the switching frequency and duty ratio of the switches.

Based on the design of the SMC-E unit ($C = 2000\mu F; R = 0.15\Omega$), the equivalent resistance, R_{eq}, is calculated for various cases of the switching frequency and duty cycle. The results are plotted in Fig. 4.29(a) for illustrative purposes. It is clear to observe that R_{eq} is strongly dependent on the switching frequency. If the switching frequency is reduced, R_{eq} is significantly increased. The impact of the duty cycle on R_{eq} is weak where the increment of R_{eq} is small by duty change. Therefore, it is concluded that regulating the branch impedance by the switching frequency is more effective.

In the proposed equalization structure for parallel connected battery modules, the SMC-E units can serve as a controllable resistor between the module and DC bus as in Fig. 4.29(b).

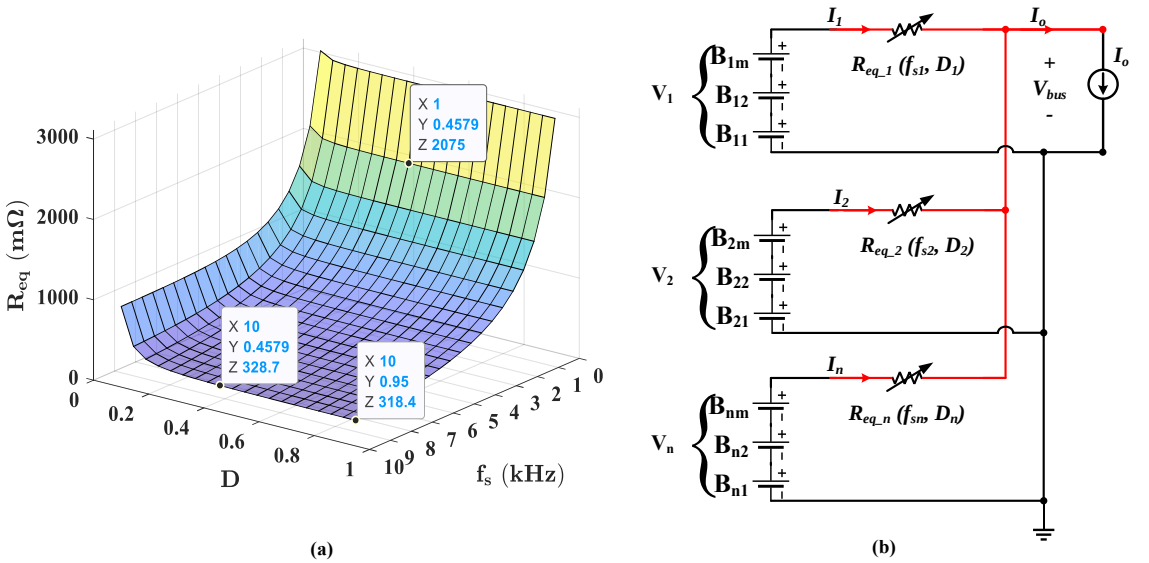


Fig. 4.29 Module equalization strategy in non-IDLE modes: (a) R_{eq} vs. f_s and D; (b) Equivalent circuit using R_{eq} model.

Therefore, in the non-IDLE mode, if the module voltages are monitored, the the following two actions can be taken.

- In the charging process, the switching frequency of the highest voltage module is reduced to increase its impedance when the voltages of the modules are mismatched. The switching frequency will be held until the voltages of the modules are all equalized. During the operation, the voltage comparison algorithm detects the next highest-voltage module and dynamically changes its switching pattern to achieve the module equalization. When the voltage of all modules is equalized within a targeted level, the individual switching frequency is increased to the original frequency to reduce the impedance. If the duty ratio is regulated to almost unity (for example 95%), the impedance will be minimized. If the voltage deviation becomes higher than the targeted level, the equalization process is triggered again. Since the currents are individually adjusted according to the voltage levels all modules can be fully charged at the same time.

• In the discharging process, the mechanism is almost similar to the charging process. However, a lower switching frequency is set for the lowest voltage module and the branch impedance is maximized. Therefore, the other modules will be discharged by a higher current. If the module voltages are all equalized, the switching frequency is returned to the original frequency with a unity duty ratio. When all modules are fully discharged, the entire process is terminated.

Cooperative Equalization Strategy for Parallel Connected Modules

In telecommunication and data-center applications, the battery system has to be always on standby to deliver the backup energy to the load. Thus, the maintenance time must be limited. In general, the modules can be equalized by the proposed method in IDLE mode. However, the balancing current is gradually reduced as the voltage deviation between the modules become smaller. Calculated balancing current and power loss of the modules are illustrated in Fig. 4.30, which supports the above statement. Therefore, the slew rate will be decreased and the equalization time is too long.

On the other hand, module equalization in the non-IDLE mode can balance the energy level of the modules by distributing the current between branches unevenly. The current distribution is controlled by the switching frequency adjustment as mentioned in Section 4.2.2. Modules have to be operated by a much higher current to achieve a high equalization speed. However, the impact of the uneven current sharing ratio on the lifetime of the battery module is not fully investigated yet.

To limit the maintenance time, the modules can be equalized in the pre-equalization period. At this stage, the cut-off voltage deviation of the equalization process can be high to utilize the high equalization speed condition of the SMC-E. After that, the algorithm in

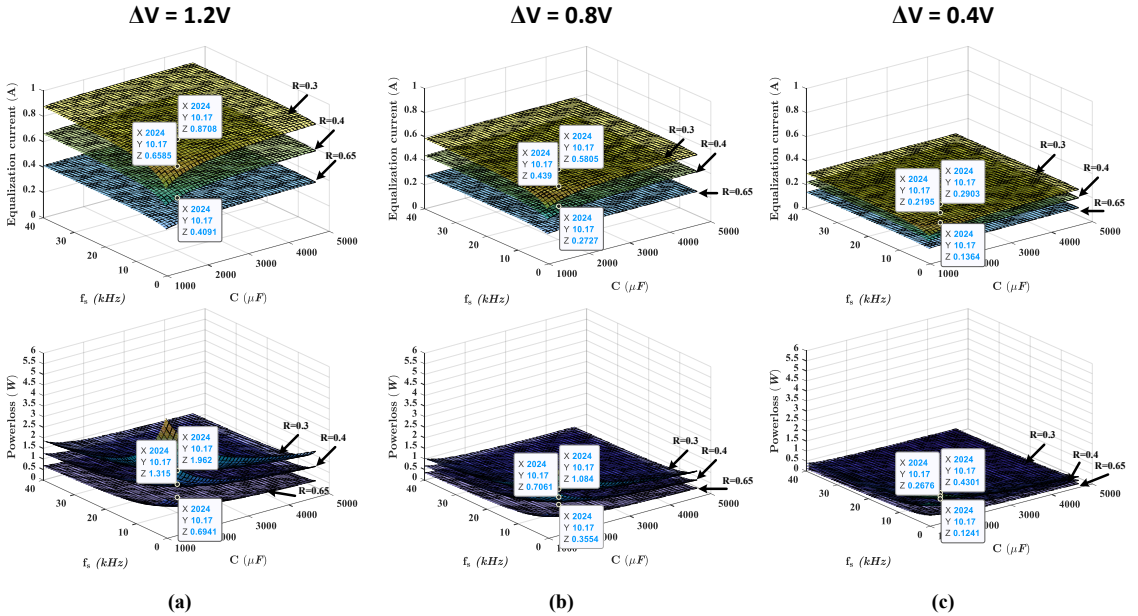


Fig. 4.30 Average current and power loss of the equalizer: (a) $\Delta V = 1.2V$; (b) $\Delta V = 0.8V$; (c) $\Delta V = 0.4V$.

non-IDLE mode is triggered to connect the modules to the DC bus. The energy levels of the modules will be gradually equalized during their operation. As a result, the energy inside the modules will be fully utilized.

The combined equalization strategy can also be useful in the hot-swap process, where the faulty battery modules are replaced by healthy ones. The newly-replaced module should have a similar energy level as the existing module to prevent the possible inrush current caused by the voltage difference. It means that the module equalization is essential for the hot-swap process.

4.2.3 Performance Verification

The module equalization strategy is implemented by a hardware-in-the-loop RTSS platform for four parallel-connected battery modules, which consist of 4 series cells in each module. In

Table 4.3 TEST SETUP ON RTSS FOR PARALLEL CONNECTED MODULES

Parameters	**Setting**		
	IDLE	**Charging**	**Discharging**
C	$2048\mu F$		
Duty ratio	$45\% - Deadtime\ \ 5\%$		
Fast f_s	$10kHz$		
Slow f_s	$1kHz$		
R_{loop}	0.15Ω		
Battery module	4S1P module of 18650 cell (3.6V/2.6Ah)		
Initial SOC of Module #1∼#4	100, 80, 90, 70%	15, 40, 20, 30%	100, 80, 90, 70%
Operation parameter	$I = 0$	$CC/CV - 4A/16.8V$	$CC - 4A$

the tests, the energy of the series cells inside each module is equalized before the parallel equalization is executed. The circuit parameters of the SMC-E unit are summarized in Table 4.3, which are similar to the design in the series-connected modules case.

Equalization During the IDLE Mode

In the IDLE mode, where there is no current flow through the modules, all modules are separated from the DC bus for the voltage scanning process. After the scanning, the highest voltage module and the lowest voltage module are detected. Hence, their module equalization strategies are executed by a fast switching frequency ($10kHz$). The equalization process is terminated after $3.5h$ and the performance of the equalization strategy is assessed in view of equalization capability and speed.

The operating profiles of the modules are illustrated in Fig. 4.31. The module voltages are equalized within $150mV$ from an initial voltage deviation of $1.25V$ after $3.5h$. Furthermore,

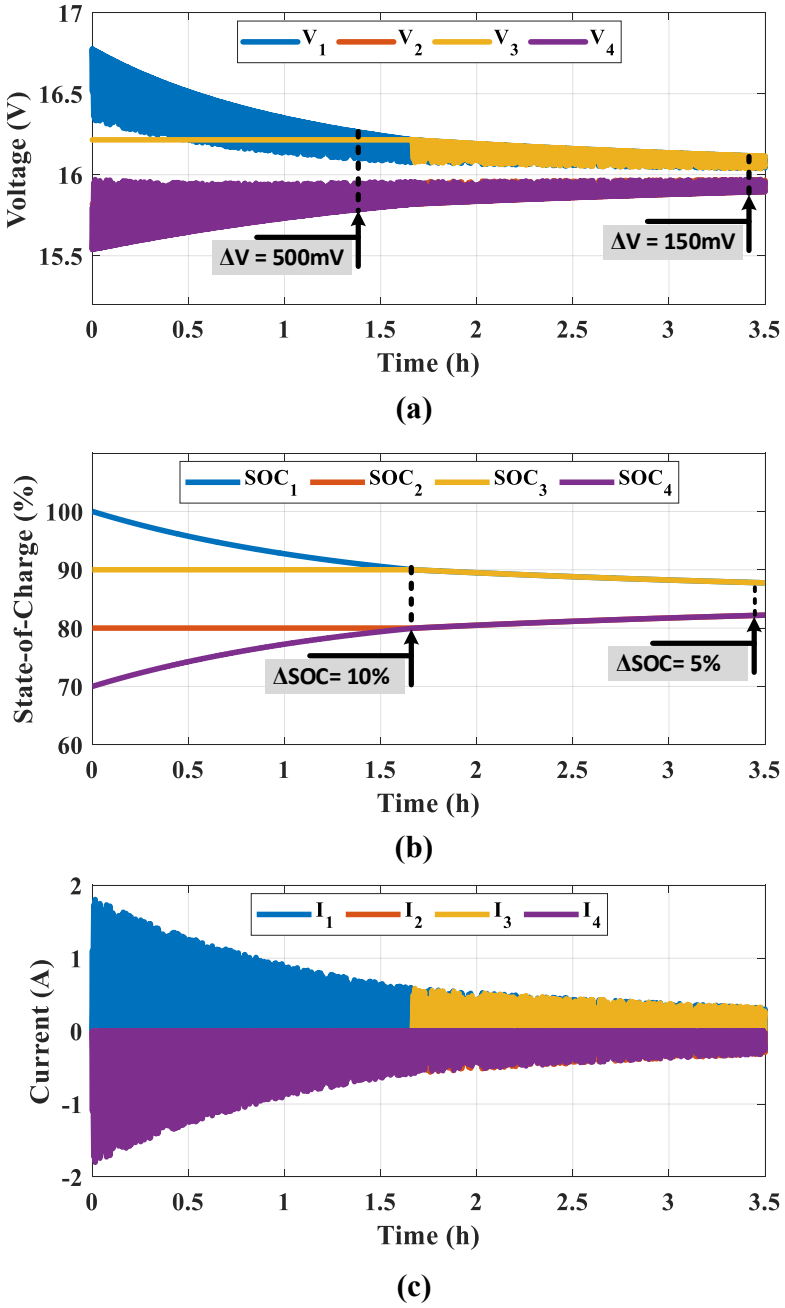


Fig. 4.31 Operation profiles of the battery modules during IDLE mode: (a) Voltage profile; (b) SOC profile; (c) Current profile.

it shows a SOC deviation of 4.82% at the end of the equalization in Fig. 4.31(b). The calculated slew rates of the voltage and the SOC equalization are $315mV/h$ and $7.2\%/h$,

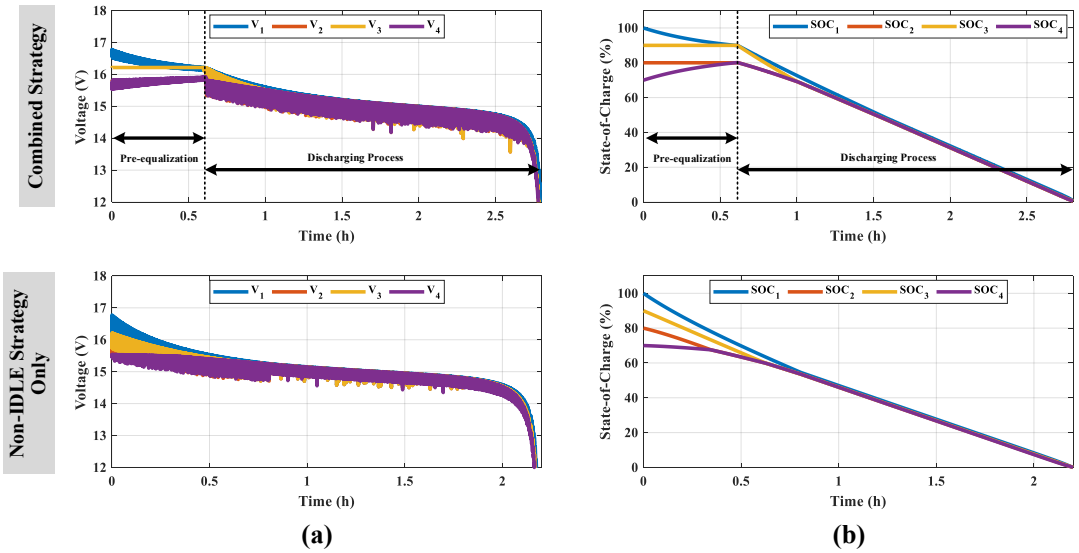


Fig. 4.32 Operation profiles of the battery modules during Discharging process under Combined strategy and non-IDLE only strategy: (a) Voltage profile; (b) SOC profile;

respectively. The equalizing speed is high at the beginning of the process, but the overall equalizing speed becomes significantly lower as the voltage deviation decreases.

In fact, the equalizing process is still under the way, but the balancing current becomes extremely low and the further equalizing process is taking a lot of time. On the other hand, the current profile in Fig. 4.31(c) reflects the equalization strategy in IDLE mode. Because modules #1 and #4 are the highest-voltage modules and the lowest-voltage modules, the equalizing process is only executed between them. After $1.65h$, the voltage of module #1 is equalized to module #3 while module #2 is equalized with module #4. Thus, the controller will alternately swap the switching pattern between modules #1-#3 and modules #2-#4 to maintain their equalizing condition. The modules are equalized one by one and the equalization level II can be achieved.

Equalization During Discharging Process

For the test of the discharging process, the same modules are connected to a $4A$ CC load. The test starts when the initial SOC levels of the modules are 100, 80, 90, and 70%, respectively. When any module reaches the cut-off condition, the entire process will be terminated.

In the discharging process, two equalizing strategies are implemented, including a combined strategy and a non-IDLE-only strategy. As mentioned, the combined strategy equalizes the modules within a target level before the discharging process is triggered. According to Fig. 4.30, the module equalization achieves the high speed when the voltage deviation is larger than $400mV$ or 10% of SOC difference. For instance, the discharging process will be triggered once the modules are equalized by the equalization strategy for the IDLE mode during the pre-equalization process. Once the voltage deviation becomes lower than V_{set} the modules are continuous discharged until the end of the discharging process in the non-IDLE mode. The voltage and SOC profiles of the modules are illustrated in Fig. 4.32, which show an effective performance of the proposed method. The modules are equalized during 0.6h and the modules are fully discharged after 2.2h. The calculated DoSE and DoVE are higher than 98%, when the module levels are equalized within a SOC difference of 1%.

It is assumed that the modules are discharged without the pre-equalization process, the module equalization strategy for the non-IDLE mode is triggered directly. By distributing the current unevenly, the energy levels of the modules are equalized within 1% of SOC difference and be maintained to the end of the discharging process. The total discharging time of this strategy is 2.1h. Compared with the combined strategy, the non-IDLE-only strategy consumes more energy.

To assess the advantages and disadvantages of both equalization strategies, the current profiles of the modules are illustrated in Fig. 4.33. The current profile in Fig. 4.33(a) reflects three stages of the combined strategy including the pre-equalization stage, the unequal discharging stage, and after the equalized discharging stage. At 0.6h point, the operation pattern is switched from the pre-equalization process to discharging process. Because the energy levels of the modules are still mismatching, the controller reduces the switching frequency of the lowest voltage module to slow down its discharging process. When the energy level of all modules is equalized at the 1.5h point, the switching frequency of all SMC-E units are set to the high switching frequency and high duty cycle to distribute the load current evenly. During the discharging process, if the controller detects the inconsistency between the modules, the frequency is adjusted again to maintain the equalization condition. In the non-IDLE-only strategy, the operating current of module #1 is quite higher than the others. The combined strategy can mitigate the over-current issue.

To illustrate the operating principle in the pre-equalization stage and the discharging stage, the detailed waveform of the battery current is captured and shown in Fig. 4.34. In the pre-equalization stage in IDLE mode, only two modules are equalized at a time as in Fig. 4.34(a). When the energy levels of the modules become almost equal to each other, the switching pattern is dynamically changed by the scanning and detecting process. As a result, the energy level of all modules is equalized. In the discharging stage, the switching frequency of the lowest voltage module is decreased. Thus, the amount of charge that flows out of the module #2 is lower than the others. Therefore, equalization level II can be achieved by the current distribution scheme.

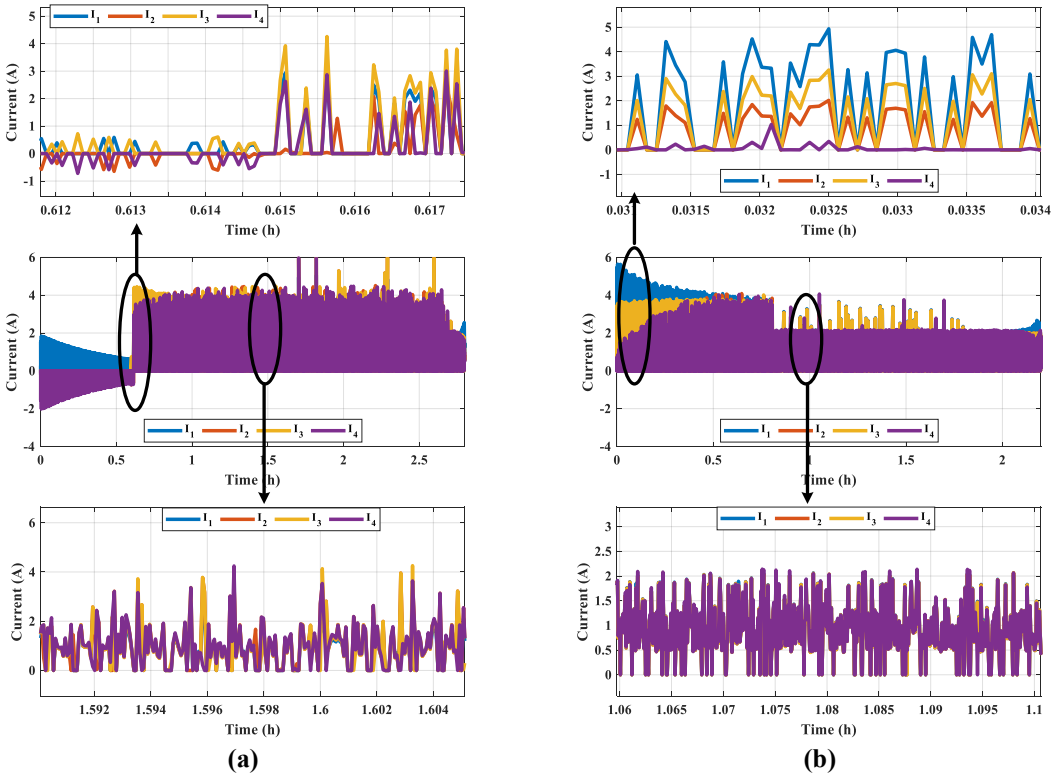


Fig. 4.33 Current profiles of the battery modules during the Discharging process under: (a) Combined strategy; (b) non-IDLE-only strategy.

Equalization During the Charging Process

For the test of the charging process, the same modules are charged by a 4A/16.8V CC-CV charging method. The initial SOC levels of the modules are 15, 40, 20, and 30%, respectively. The entire process will be stopped if any module achieves the fully charged condition. Similar to the discharging process, two equalizing strategies can be implemented. Since the charging current can be managed, the non-IDLE-only strategy can operate well without any over-current issue. The operating profile of the modules is presented in Fig. 4.35. It is observed that the energy levels of the modules are equalized within a SOC deviation of 1% after $1.5h$ and all modules are fully charged at the same time. The current profile in Fig. 4.35(c) shows a strategy switching at time point $1.5h$, the switching frequency of all SMC-E units of all

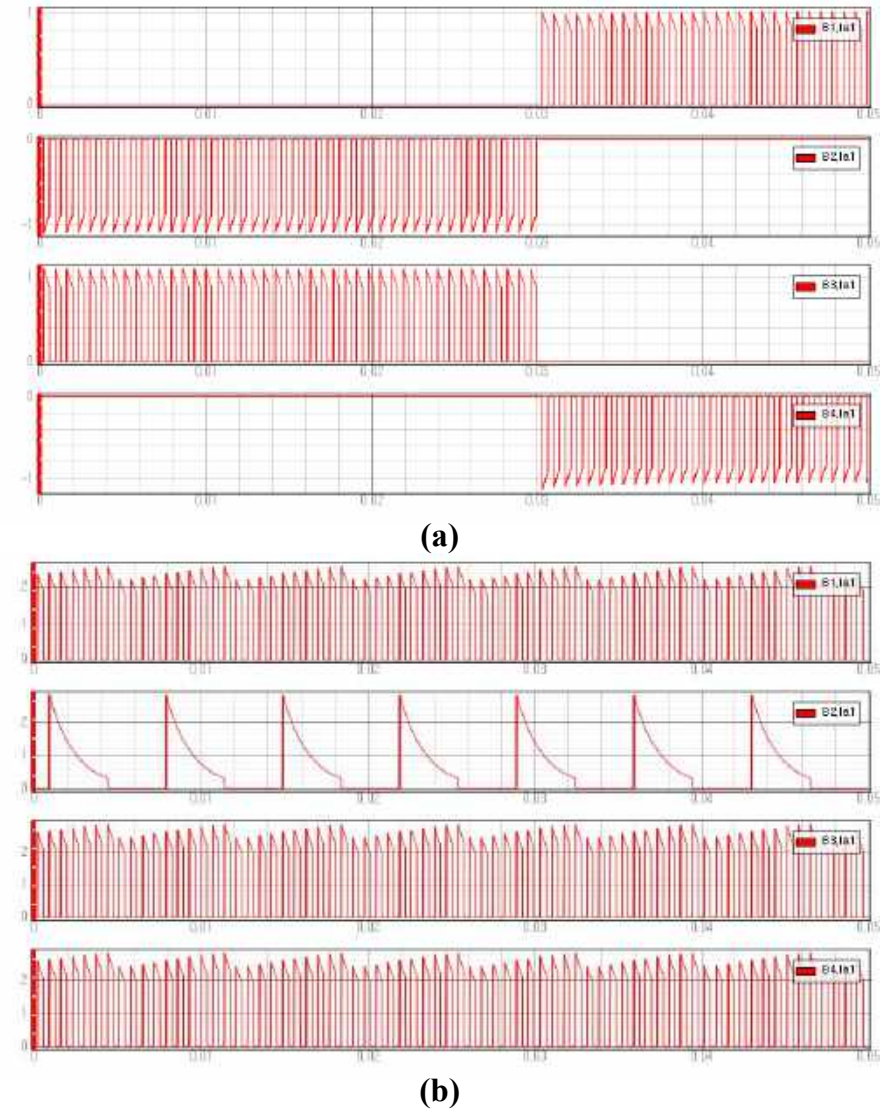


Fig. 4.34 Current waveform of the battery modules during: (a) Pre-equalization; (b) unequal discharging/charging process.

modules is switched to the same frequency and duty ratio to distribute the load current evenly. In addition, the DoVE and DoSE of the proposed method in the charging process can achieve 98% at the end of the charging process. Vividly, the proposed modular equalization strategy shows high effectiveness to mitigate the inconsistency issue at the module levels.

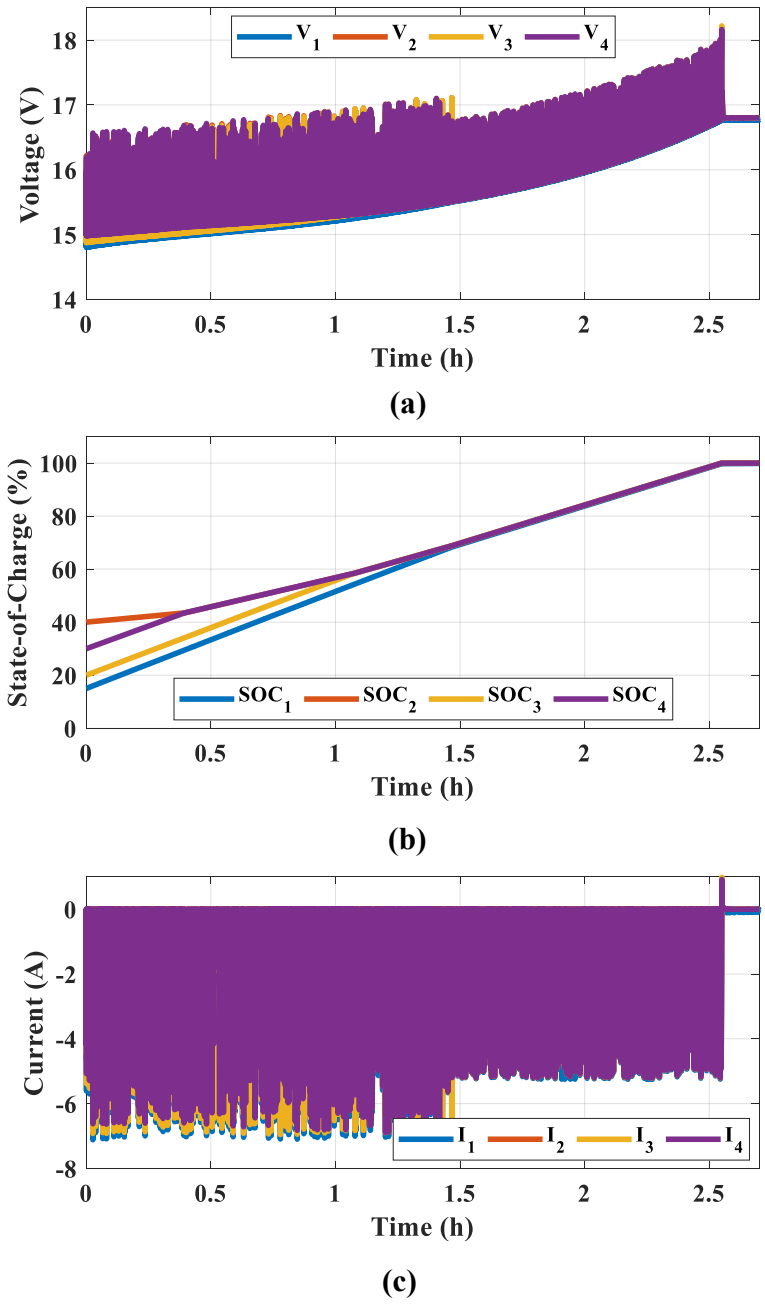


Fig. 4.35 Operating profiles of the battery modules during Charging process: (a) Voltage profile; (b) SOC profile; (c) Current profile.

4.3 Conclusion of the Chapter

In this Chapter, the extension of the SMC-E unit for the module equalizing strategy of series and parallel connected modules is proposed. In the series connection, two control equalizing strategies are proposed to increase the equalizing speed. The hybrid strategy has a 13.5% faster speed than the conventional method. Although the autonomous strategy has a lower speed than the hybrid strategy, the process won't require any sensing circuit which can reduce the size and cost of the system.

In addition, the same design of the SMC-E unit can be applied for the parallel-connected system. The equalizing strategy is proposed for three types of operations, including the IDLE mode, the charging process, and the discharging process. In all operations, the energy levels of the modules are equalized with high performance. The scheduling algorithm can be combined with the proposed strategy to further improve the equalization speed and increase capacity utilization.

Chapter 5

Conclusion and Future Works

5.1 Conclusions

This thesis presents equalization strategies for modular battery energy storage systems in order to mitigate the inconsistency in the cell-level and the module-level characteristics. The performance of equalization strategies is verified through various test scenarios and design parameters. From the results, the principal contributions of this thesis are summarized as follows:

• Firstly, a novel SMC-E structure is proposed. The principle of operation of the SMC-E is analyzed in order to optimize the design. Additionally, the design guidance for the switching matrix structure, gate driver circuit, and sensing circuit is provided. An optimal pairing algorithm is proposed to achieve the highest equalizing speed without the co-operation of the BMIC circuits.

• Secondly, a unified average model (UA-model) is proposed to accelerate the simulation of the equalizing system over the long term. By implementing the UA-model for the performance

evaluation, different topological configurations of the equalizers can be assessed and compared within a short time.

• Thirdly, the SMC-E unit is executed for the module equalizing feature. Two equalization strategies are introduced to simultaneously achieve the equalization levels I and II of the series-connected modules. The hybrid strategy shows a high equalization capability for the cells and the modules while the autonomous strategy can be operated without the guidance of any sensing circuit.

• Fourthly, the SMC-E is also applied for the modules connected in parallel. Two equalization strategies are proposed based on the energy exchange and the current distribution scheme. In the IDLE mode, the energy exchange scheme is used to transfer energy from the high-level module to the low-level module. In the non-IDLE mode, the branch currents are distributed unevenly to balance the energy level of the modules. Once the equalization condition has been reached, the branch currents are evenly distributed to minimize the loss.

• Finally, the performance of the modular equalization strategies is verified by hardware-in-the-loop-based RTSS and experimental results.

5.2 Future Works

Besides the work that has been done in this thesis, some unexplored subjects may be considered as future studies. The potential topics can be suggested as

• A family of switch-matrix energy tank (SMET-E) can be developed along with SMC-E in order to improve the equalization performance. The promising topology can be switched LC resonance converter and resonant switched capacitor converter.

• The online voltage monitoring function can be integrated into the hardware of the SMC-E unit since the balancing capacitor can be connected to any cell through the switch-matrix.

• By the same token, an online measurement of cell impedance can be integrated into the existing SMC-E hardware as a symbiosis system, where it is expected that the impedance of each cell will be estimated individually.

• The SMC-E can replace most part of the existing BMIC circuit since it can provide similar features to the BMIC.

• Under the current distribution scheme, the equalization strategy for the parallel-connected modules has the potential to equalize not only the SOC levels but also the SOH levels of the second-life battery modules.

• When the advanced equalization method is adopted, the overall lifetime of the battery pack can be improved. However, the impact of the equalizer on the lifetime improvement should be investigated. By cycling the battery pack with and without the cooperation of various equalizers, the lifetime improvement can be assessed. It is expected that the equalizer has high efficiency with lower loss will slow down the inconsistency evolution of the cells.

• Since the SMC-E focus to equalize the voltage level of the cells, the battery aging is not considered yet. However, the capacity, impedance, and OCV-SOC characteristic of the cells can be heterogeneous in the actual situation. Thus, the impact of the mismatch aging condition on the performance of the SMC-E should be investigated.

Biography

Phuong-Ha La received a B.S. degree in automation and control systems from the University of Technology - National University of Ho Chi Minh City in 2014. From 2013 to 2017, he worked for Dien Quang lamp JSC. as an *R&D* and project management specialist. Now he is working toward a Ph.D. degree at the University of Ulsan - Energy Conversion Circuit Laboratory.

His research interests include battery management systems, battery chargers, cell balancing circuits, and symbiosis equalizing-state estimating system.

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Journals

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Switch-Matrix Active Equalization Strategies for Modular Battery Energy Storage System

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Energy Conversion Circuit Laboratory

Agenda

1. Introduction and Research Motivation
2. Switch-Matrix Capacitor Equalizer for the Cell level
3. Novel Simulation Techniques for Performance Assessment of SET-E in Long-term Operation
4. Module Equalizer System for Series and Parallel Connected Battery Modules
5. Conclusions and Future Works

Research Objectives

❖ **Develop a novel structure of equalizer to mitigate the inconsistency in both cells and modules.**

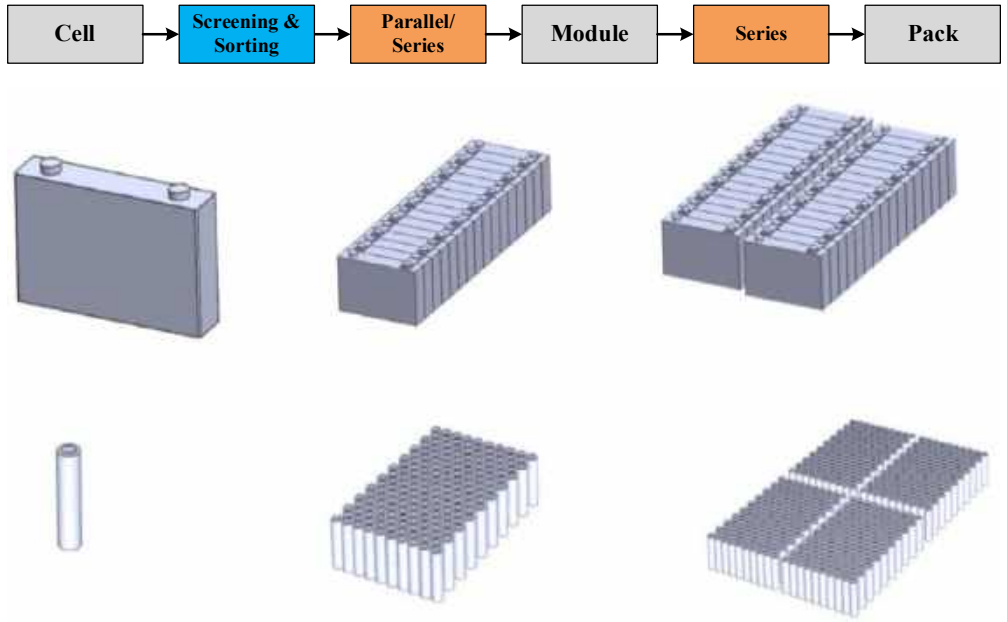
- The impact of test scenarios on equalizer performance is analyzed to evaluate the advantages and disadvantages of different topologies. As a result, a new structure based on the switch-matrix capacitor equalizer is proposed.
- A simulation method is proposed to rapidly evaluate the performance of the equalizer to speed up the development process.
- Develop a module equalizer based on the proposed SMC-E to balance energy of the series connected modules to reduce the equalization time and size.
- Develop the equalization strategies for the parallel connected modules in the IDLE, discharging, and charging process.

Agenda

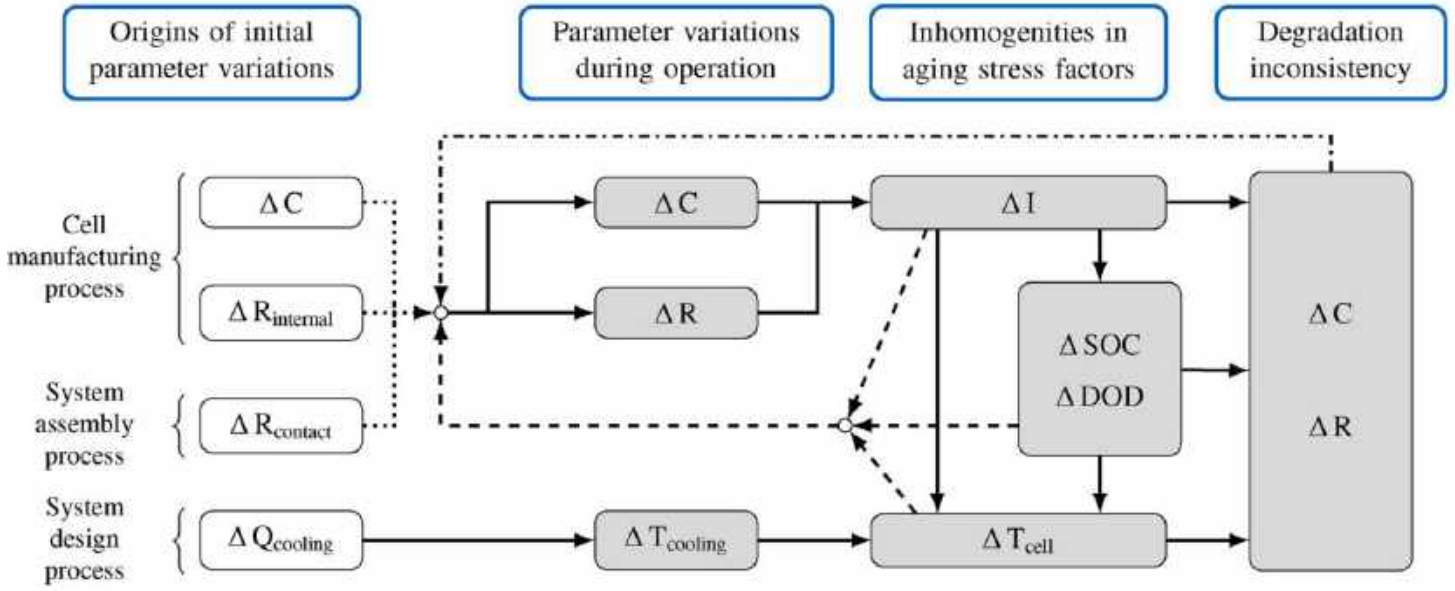
1. Introduction and Research Motivation

- ❖ Impact Of The Cell-inconsistency To The Battery Performance
- ❖ Conventional Structure Of The Battery Management System And Problem Identification

1.1 Battery Packing and the Inconsistency

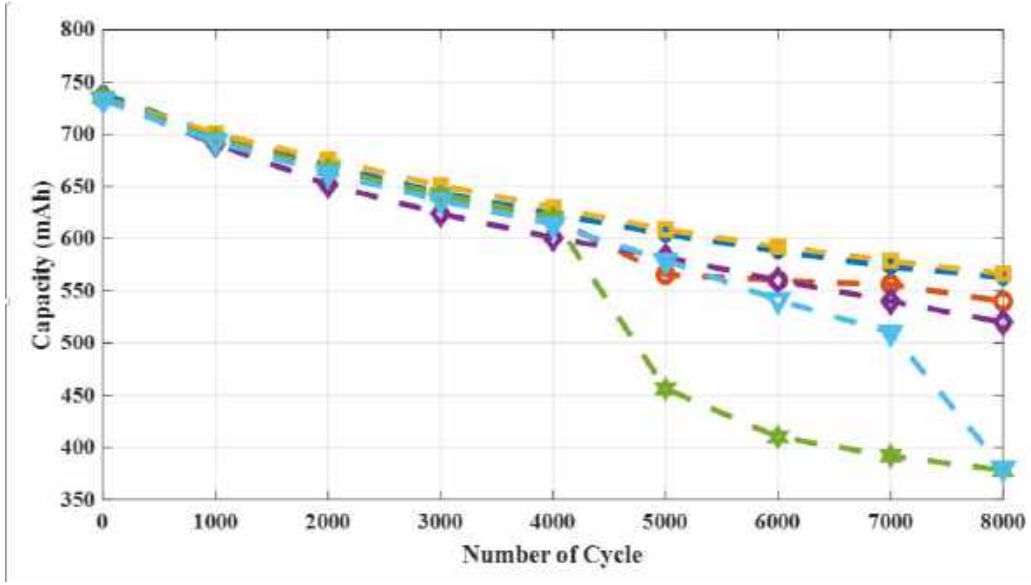


Battery packing process

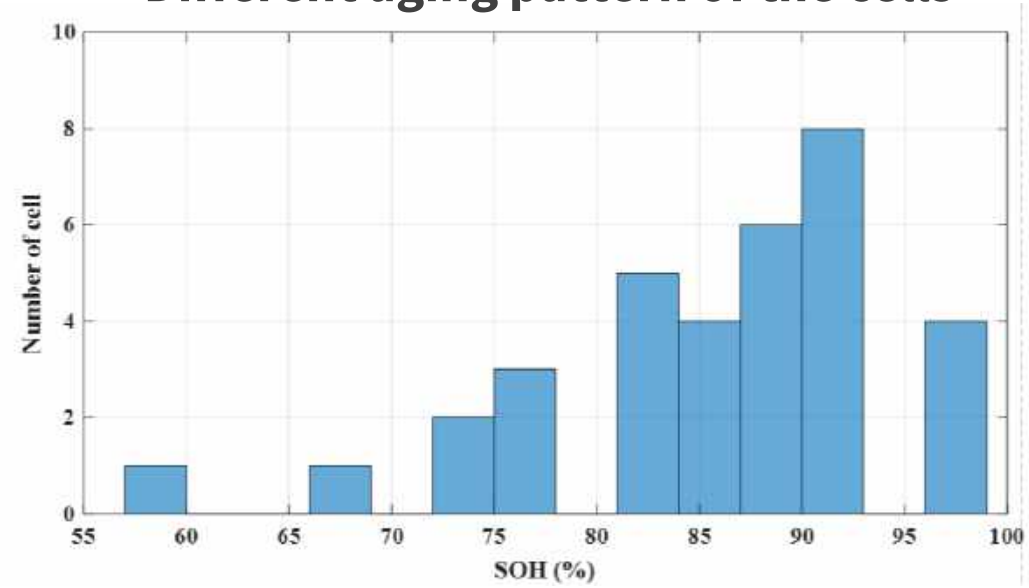


Overview of Cell-inconsistency*

*Baumann, Michael, Leo Wildfeuer, Stephan Rohr, and Markus Lienkamp. **"Parameter variations within Li-Ion battery packs–Theoretical investigations and experimental quantification."** *Journal of Energy Storage* 18 (2018): 295-307.



Different aging pattern of the cells

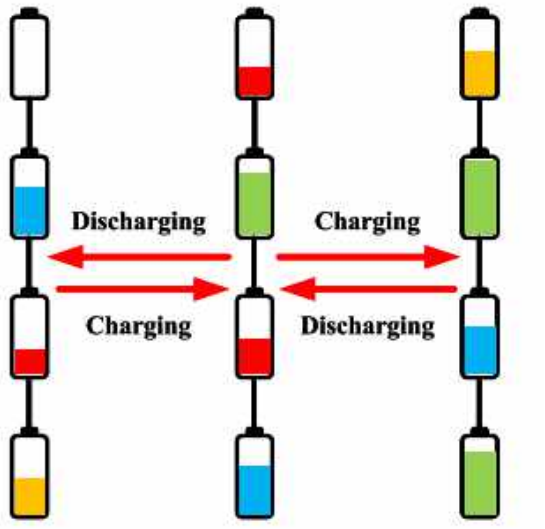


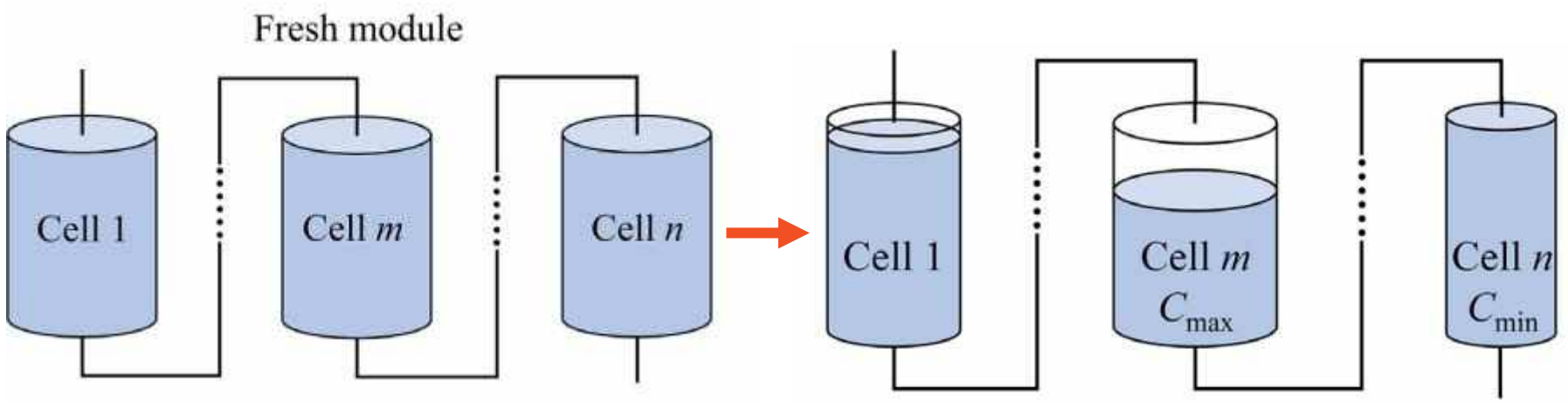
Inconsistency in retired battery pack of EV

1.2 Aging Pattern and the Cell-Inconsistency

- **Aging pattern of the cells** is different from each other because of the **tolerance of the material**.
- Even when **cells operate under the same conditions**, cell inconsistency still exists.
- There is **no link** between **capacity mismatch** and **resistance mismatch** between the cells.

1.3 Cell-inconsistency in Series Connection

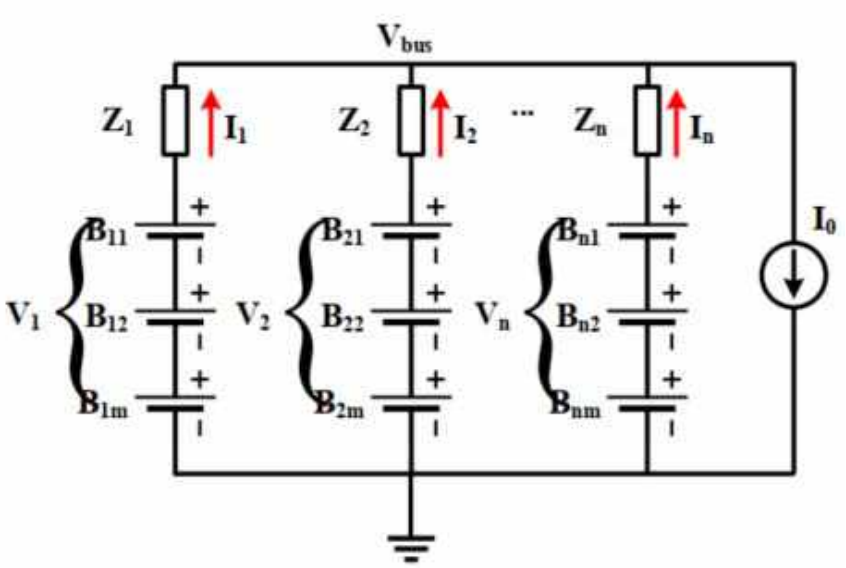




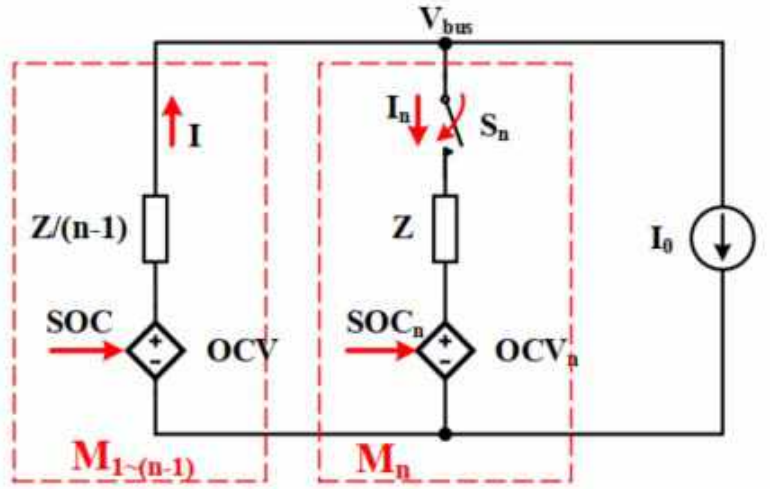
- **Cell-inconsistency without the management system** may lead the battery string to the **over-charging or over-discharging.**
- **Battery management system protects** the battery string by **terminating the operation process** when **any cell reaches the cutoff conditions**.

➔ **Cell-inconsistency increases.**

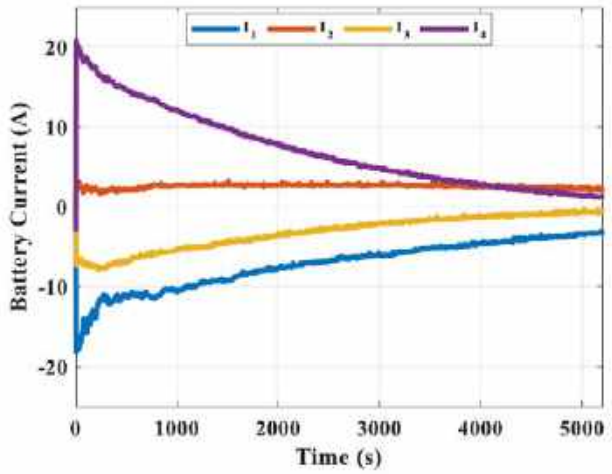
1.4 Cell-inconsistency in Parallel Connection



Equivalent circuit of Parallel connected modules



Equivalent circuit of hot-swap process



$$Z_1 I_1 - Z_2 I_2 = V_1 - V_2$$

$$Z_1 I_1 - Z_3 I_3 = V_1 - V_3$$

...

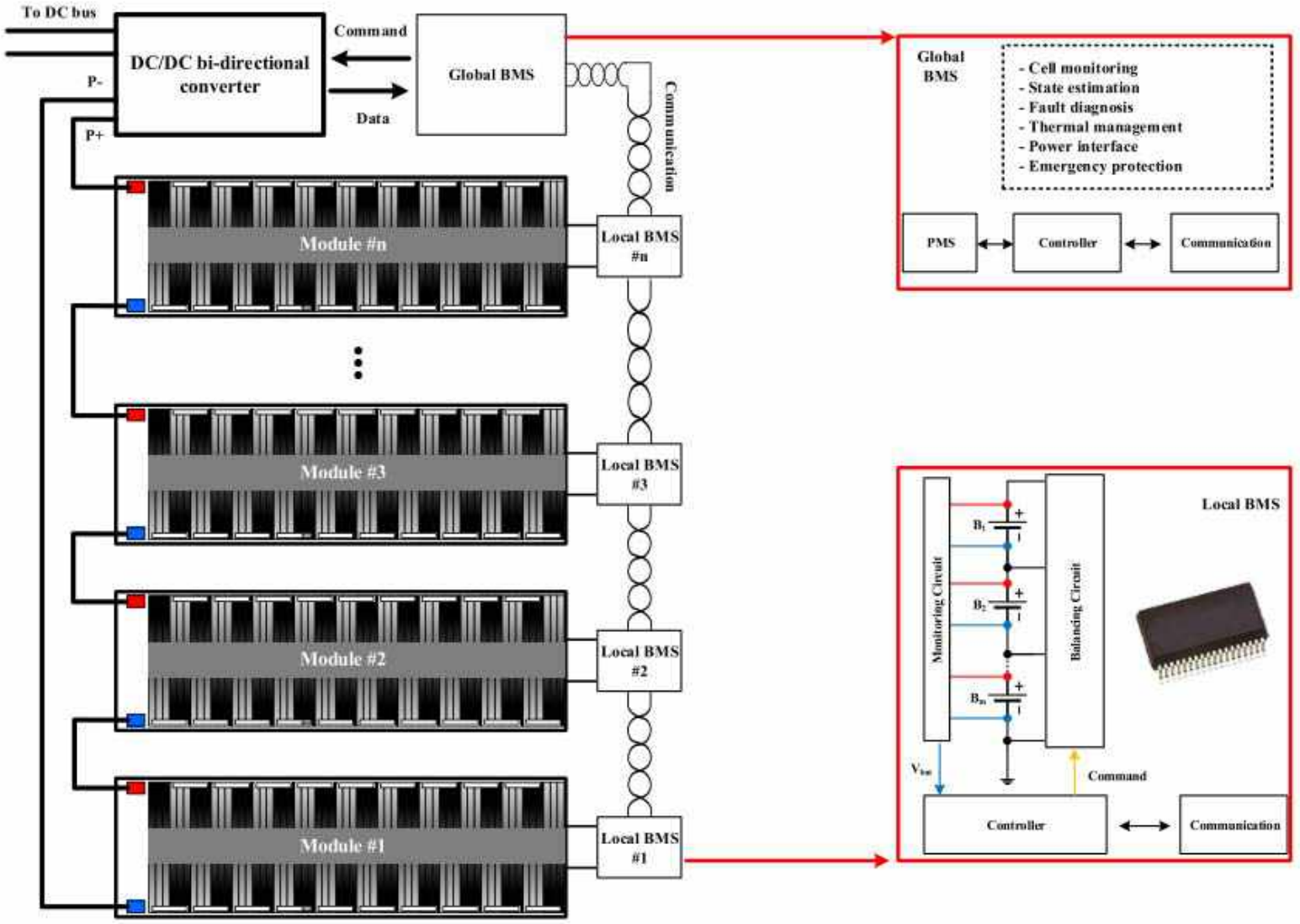
$$Z_1 I_1 - Z_n I_n = V_1 - V_n$$

$$I_1 + I_2 + I_3 + \ldots + I_n = I_0,$$

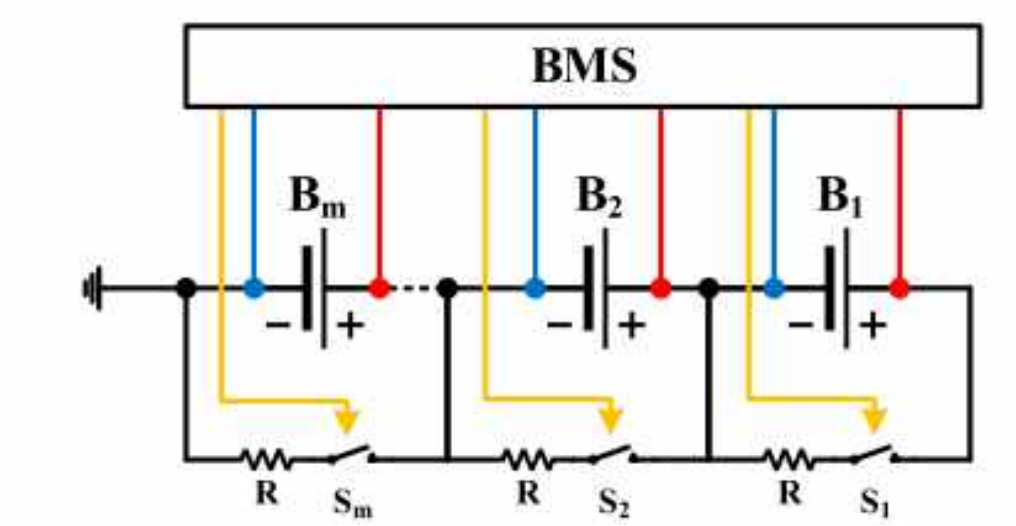
- **In a parallel connection**, the **branch currents** are **distributed depending on the relative voltage and impedance** of the cells or modules.
- Even when in **IDLE mode**, **circulating currents appear**.
- **Impact of inconsistency** becomes **more serious in hot-swap process**.

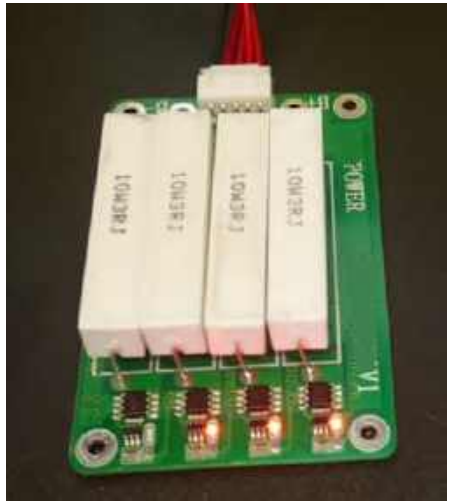
1.6 Modular Structure of the BMS

- **Battery system** is divided into **several modules** and is connected **in series**.
- **Inside a module**, multiple **cells** are **connected in series and parallel.**
- **Cells** in a module are **monitored through a sensing circuit.**



1.6.1 Equalizer Classification – Passive Methods

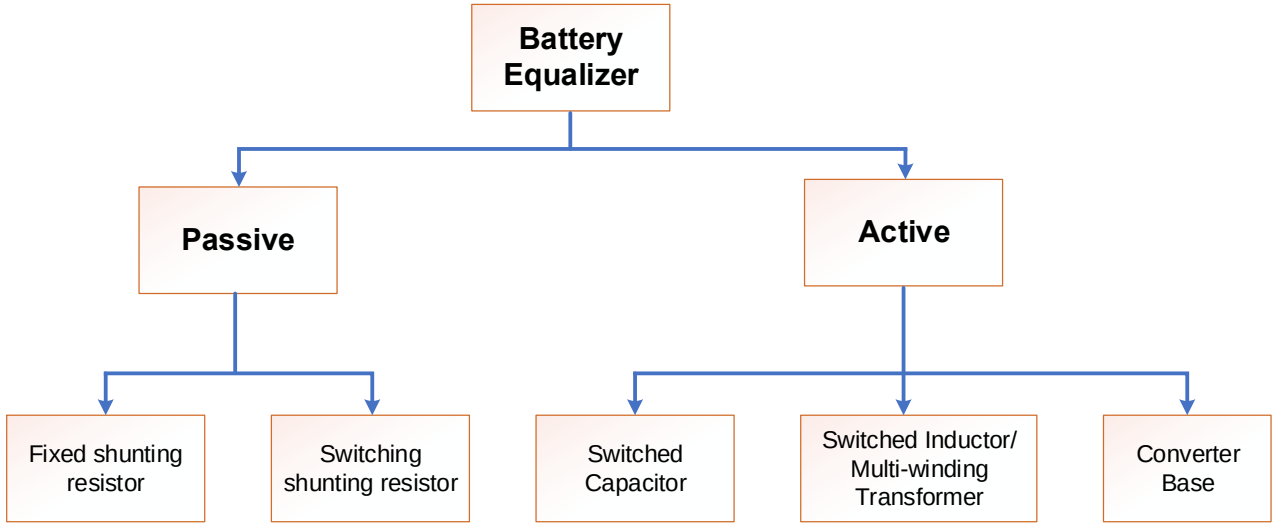


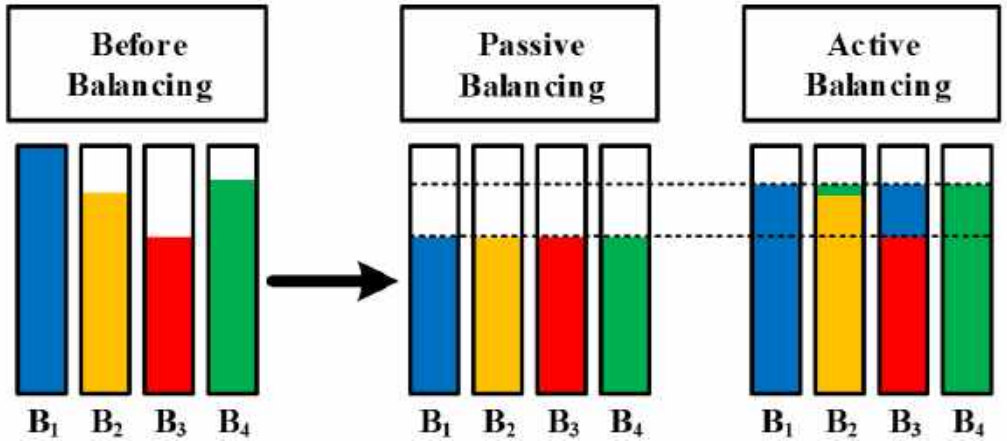


- **Passive balancing** method **dissipates the energy of the higher voltage cells** until the cell voltage becomes even.
- **Balancing current**, I_{bal}, can be designed **according to the balancing resistance**.
- To achieve a high equalizing speed, **high-power resistor is required**, and vice versa.

$$I_{bal} = \frac{V_{bat}}{R}$$

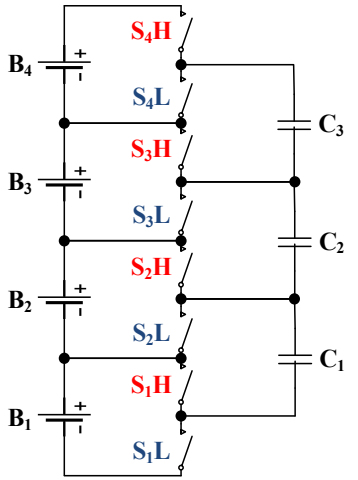
1.6.2 Equalizer Classification – Active Methods

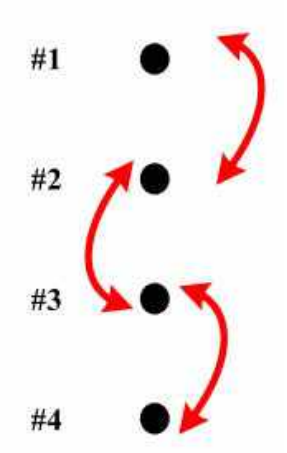


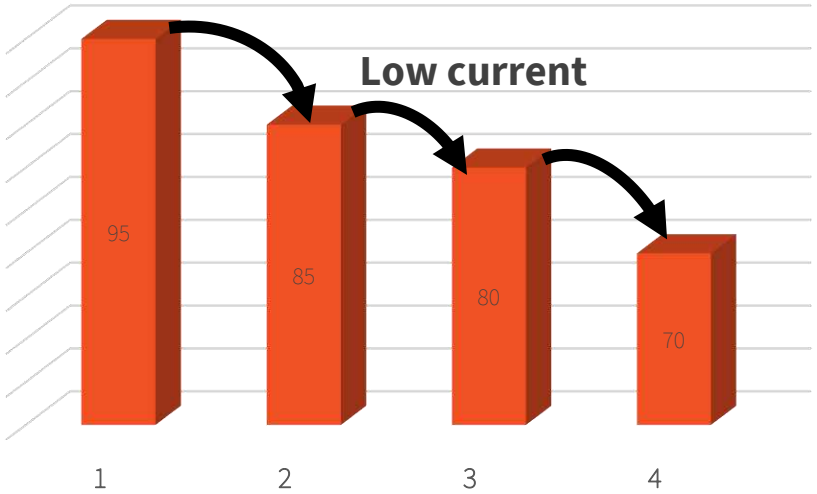


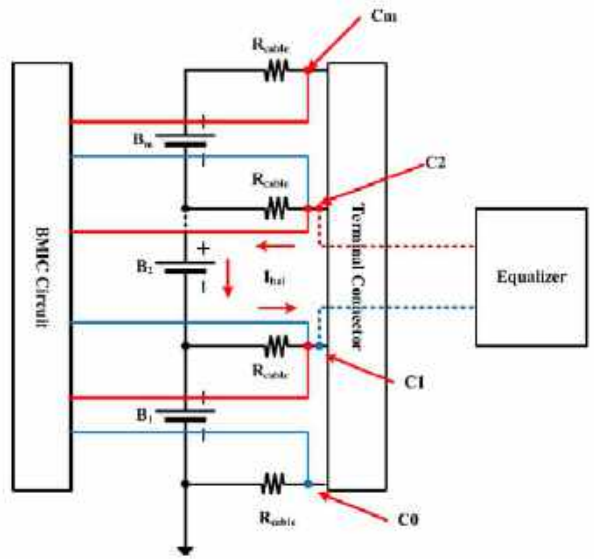
- **Active balancing methods transfer energy** from one cell to another.
- **Active balancing methods** have **more advantages** in terms of **equalization speed and energy saving**.
- **Switched capacitor equalizer** group got more attention due to **its simplicity and efficiency**.
- **Switched inductor and transformer-based methods** can achieve **a high equalization speed** but require a **complex control method**.

1.7 Problem Identification



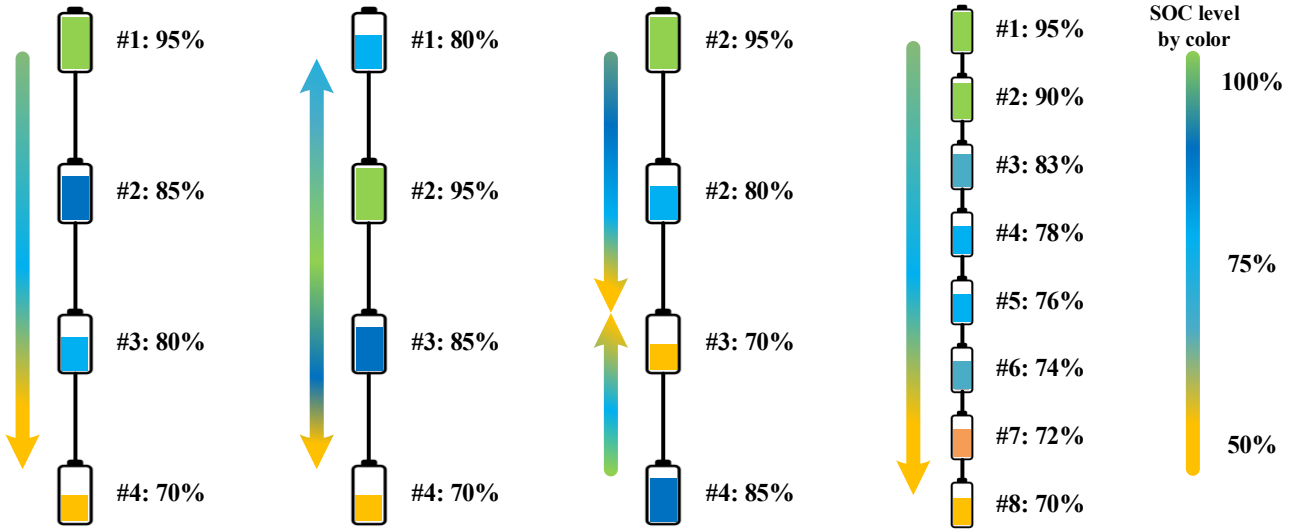


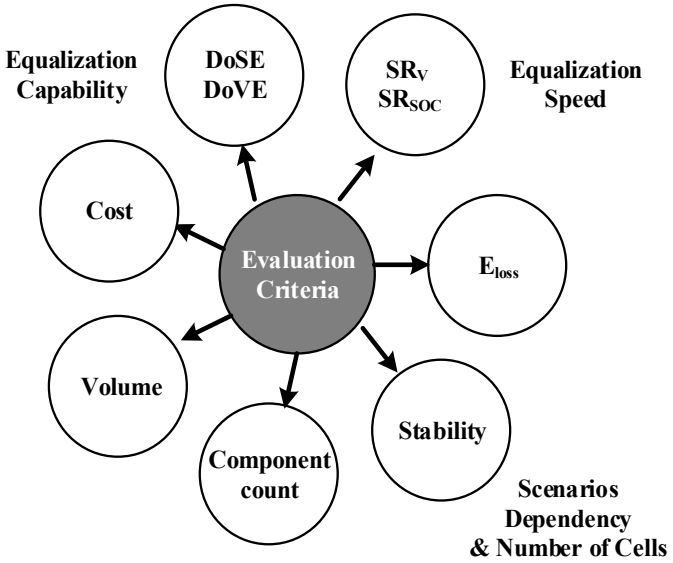




- **Autonomous control scheme** requires **many intermediate steps** to transfer energy between the **highest-level cell and the lowest-level cell**.
- Since the **amplitude of the balance current** depends on the **voltage deviation between two cells**, the **intermediate steps** have **a lower balance current** than the **directly transferring**.
- **Voltage drop** on the **resistance of the wire and connector** affects the **accuracy of voltage measurements**.

1.7 Problem Identification



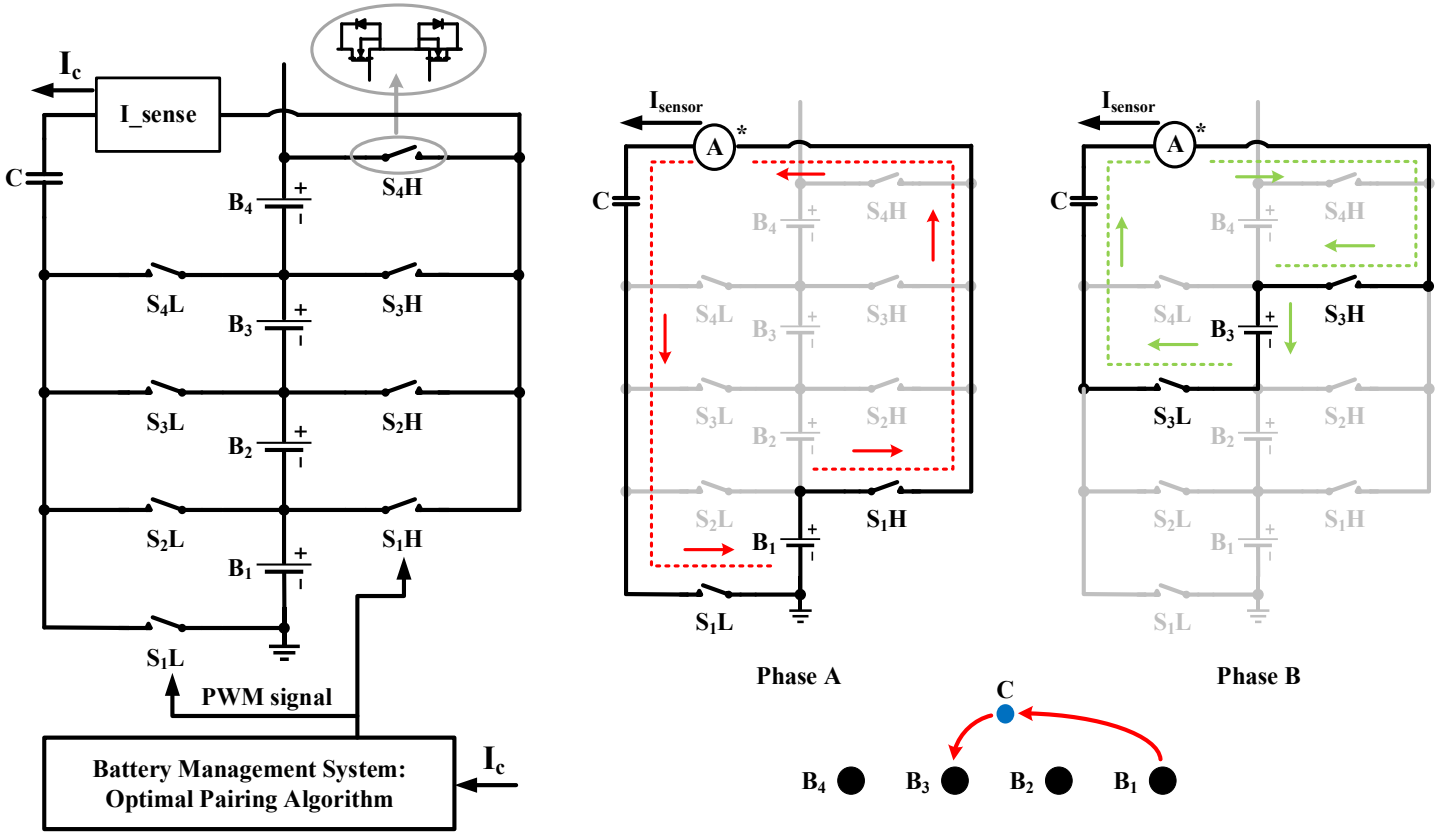


- **To compare performance of the equalizers**, tests should be performed **under the same conditions**.
- **Various evaluation criteria should be considered**, including equalization capability, equalization speed, loss, stability, component counts, volume, and cost.
- **Equalization capability, equalization speed, and performance stability** are more important.

Agenda

1. Introduction and Research Motivation
2. Switch-Matrix Capacitor Equalizer for the Cell level
   - 2.1 Proposed Topology and Operation Principle
   - 2.2 Optimal Pairing Algorithm
   - 2.3 Design Consideration
   - 2.4 Performance Verification
   - 2.5 Conclusion of the Chapter
3. Novel Simulation Techniques for Performance Assessment of SET-E in Long-term Operation
4. Module Equalizer System for Series and Parallel Connected Battery Modules
5. Conclusions and Future Works

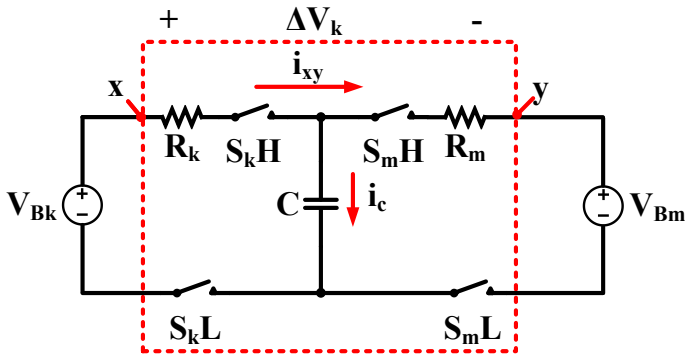
2.1 SMC-E: Topology Configuration and Operation Principle

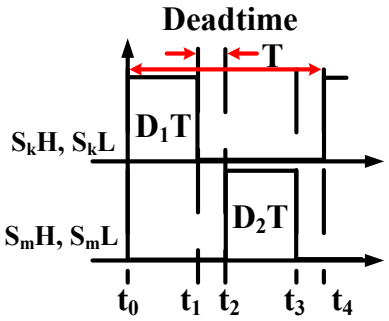


***Energy is transferred directly from one cell to another.**

- **Switch-matrix** is utilized to **directly connect any-cell to the balancing capacitor, C.**
- **A current sensor** is used to **measure the balancing current of each pair of the cells** for the optimal pairing algorithm.
- **Operation principle** is divided into **two phases:**
  - **Higher voltage cell** charges the **capacitor** in phase A.
  - During phase B, energy is transferred **from the balancing capacitor to the lower voltage cell**.

2.1 SMC-E: Topology Configuration and Operation Principle



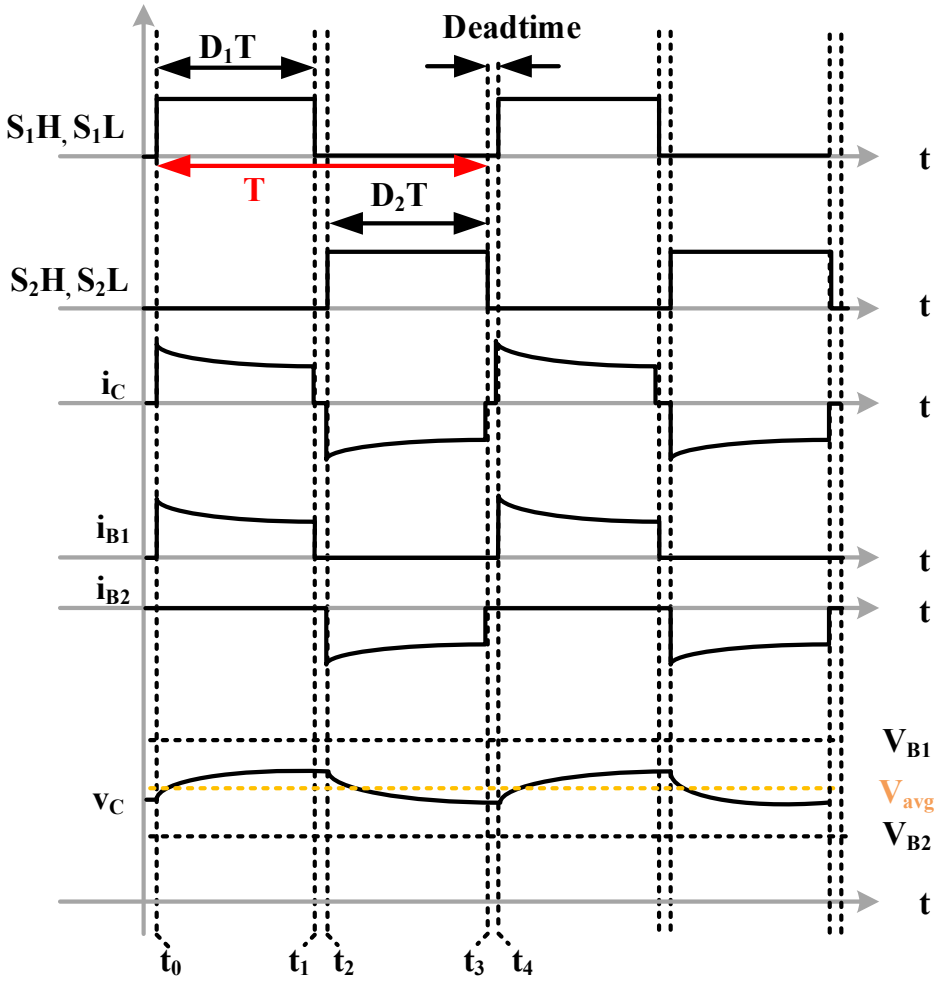


➢ **Equalization process of two** cells is reflected by **the average balancing current in phase A and phase B:**

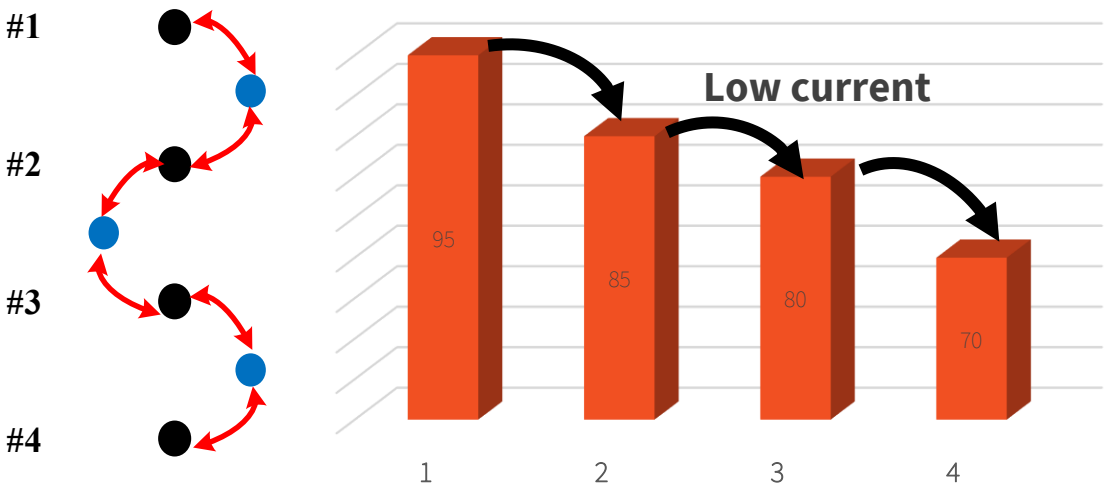
$$I_{avg1} = \frac{1}{2} C f_{sw} (V_{B1} - V_{B2}) \left(1 - exp(\frac{-D_1}{f_{sw} R_1 C})\right),$$

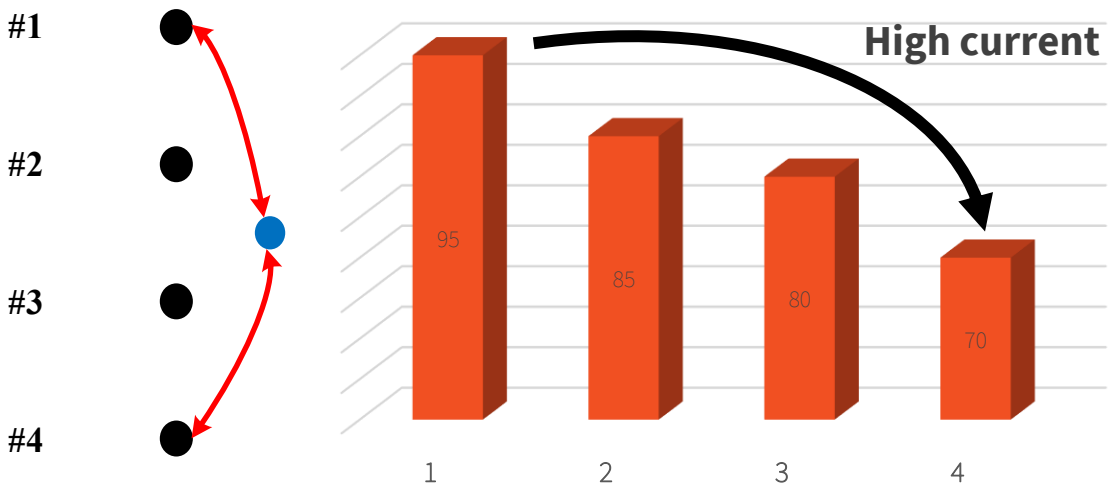
$$I_{avg2} = \frac{1}{2} C f_{sw} (V_{B2} - V_{B1}) \left(1 - exp(\frac{-D_2}{f_{sw} R_2 C})\right) exp(\frac{-1}{2 f_{sw} R_2 C}).$$

➔**A higher voltage deviation, a higher balancing current will be.**



2.2 SMC-E: Optimal Pairing Algorithm





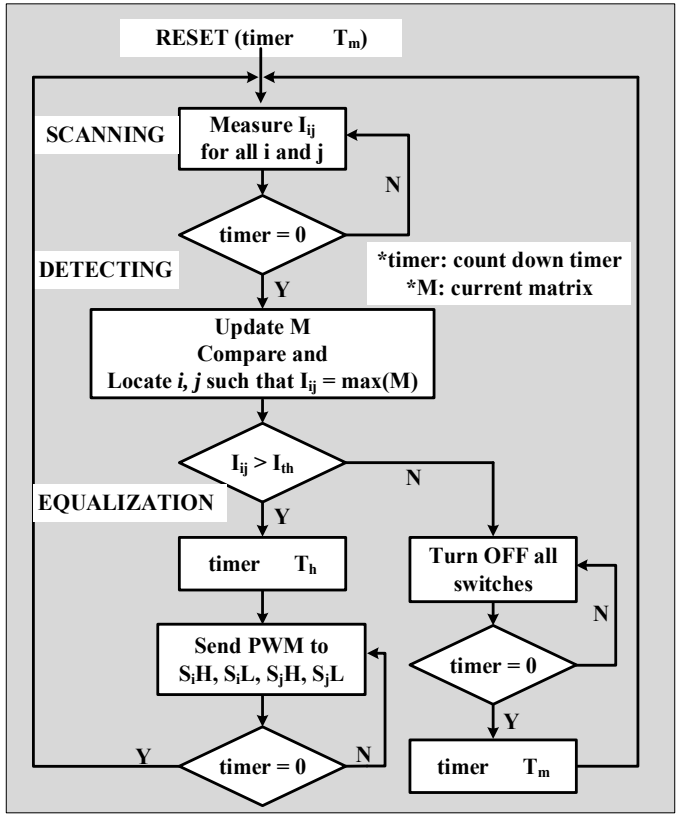
Conventional active balancing method:

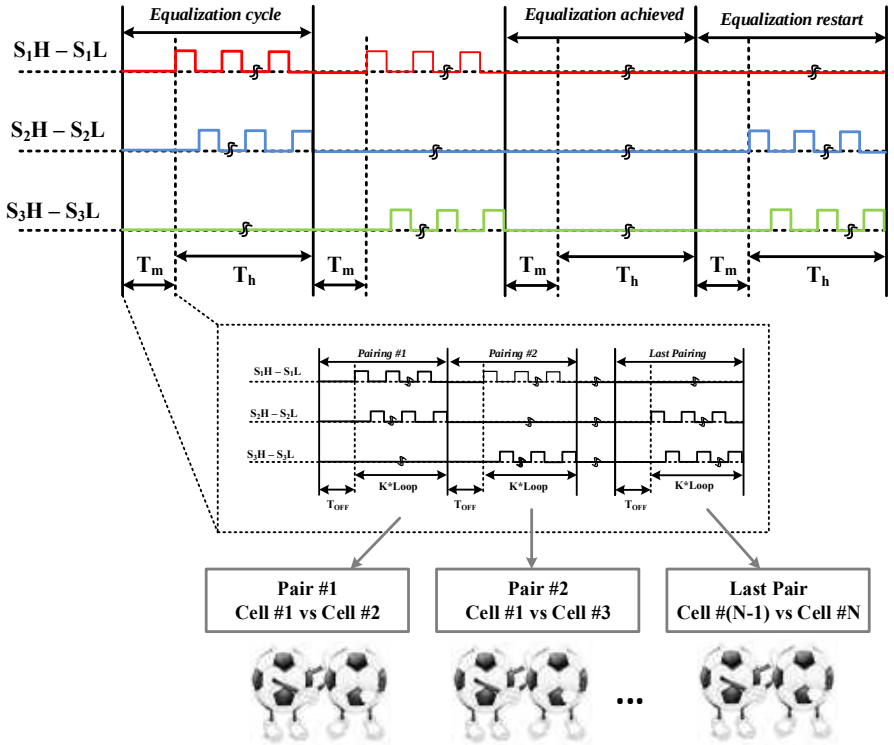
- **Energy is transferred through many intermediate step.**
- **Balancing current in the intermediate step is low due to the small voltage deviation.**

Proposed switch-matrix capacitor equalizer:

- **Energy** is **transferred directly** from **highest energy level cell** to the **lowest energy level cell**.
- **High balancing current** can be achieved which **accelerates the balancing process**.

2.2 SMC-E: Optimal Pairing Algorithm



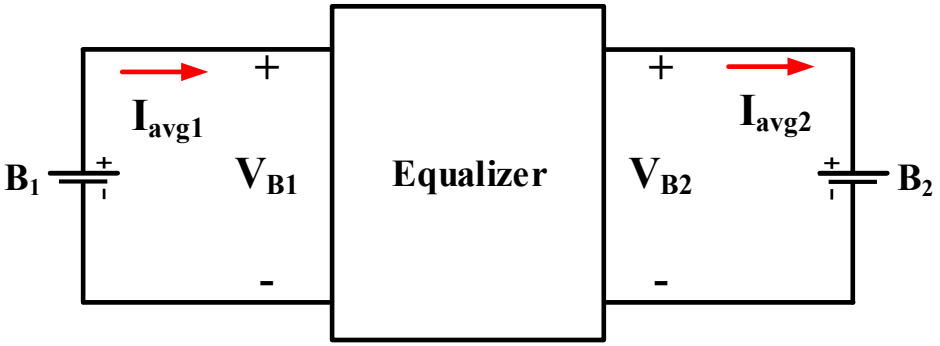


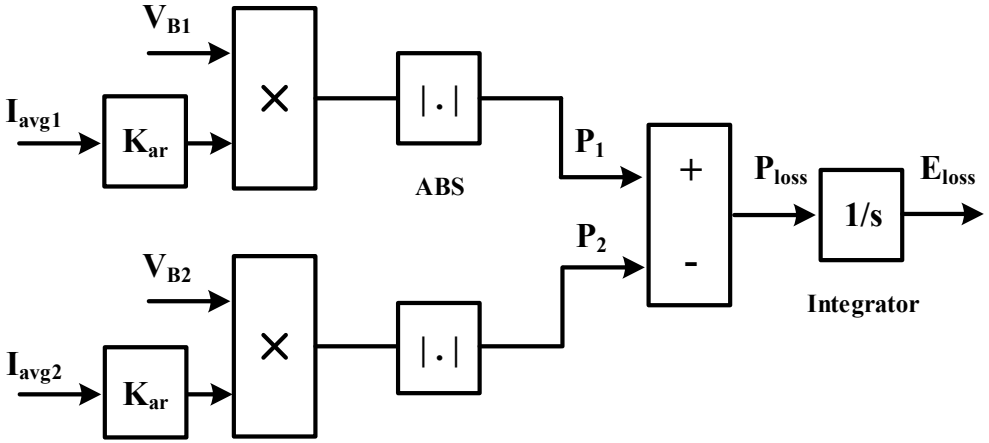
- **Equalization process** is divided into **multiple cycles.**
- **An equalization cycle** starts by the **current scanning** to **detect the max-min cell pair**.
- **Switching pattern of the max-min cell pair** is held during T_h for the **fast energy exchange speed**.
- **Equalization process is stopped** when the **optimal current is lower than I_{th},**

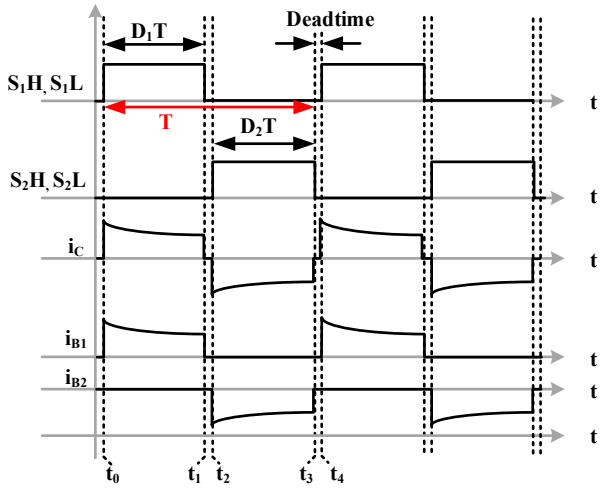
➔ **The cells are equalized.**

***Optimal pairing algorithm** is used to **detect the shortest way** for the **energy transferring process.**

2.3 SMC-E: Design Consideration – Loss Assessment







➢ **Balancing current waveform** of SMC-E is **almost pulsating**.

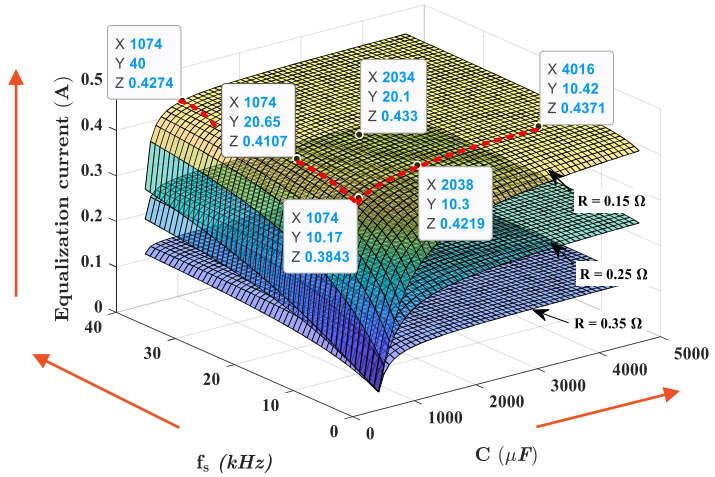
➔ **RMS current** can be **approximately calculated** based on the **average balancing current**.

$$K_{ar} = \frac{I_{RMS}}{I_{avg}} = \frac{I_0\sqrt{D}}{I_0 D} = \frac{1}{\sqrt{D}}.$$

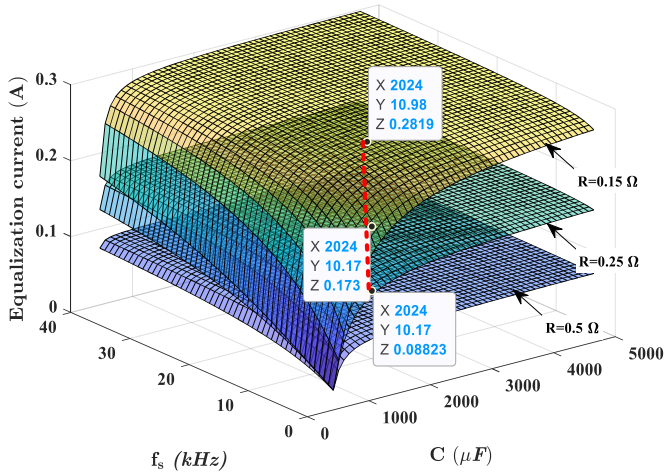
2.3 SMC-E: Design Consideration – Capacitance vs. Switching Frequency (D_1=D_2=0.45)

Internal resistance has a strong impact.

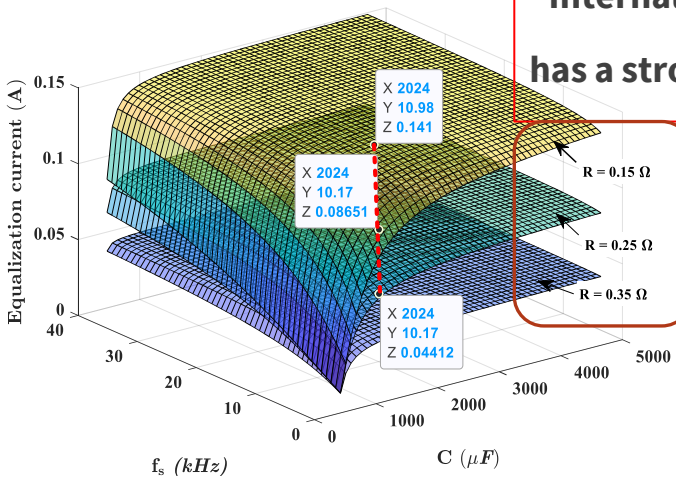
ΔV = 300mV

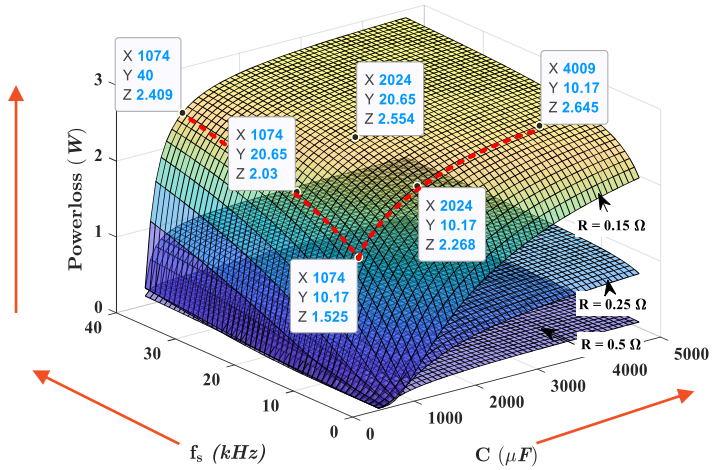


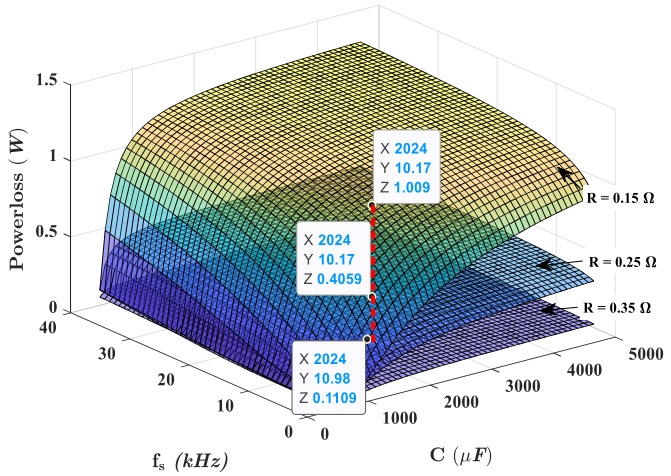
ΔV = 200mV

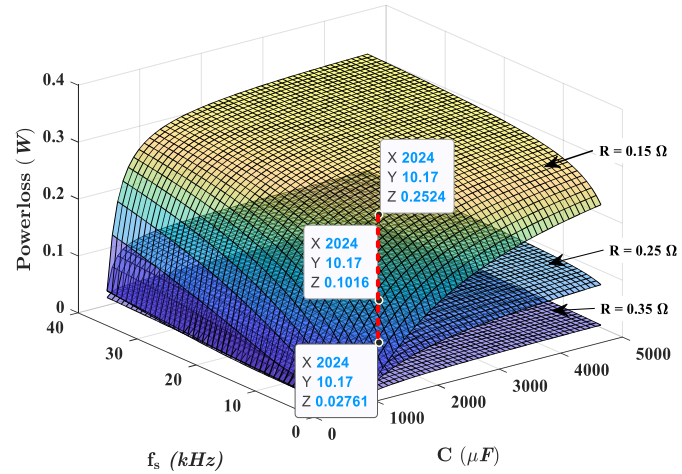


ΔV = 100mV









2.3 SMC-E: Design Consideration – Capacitor Size

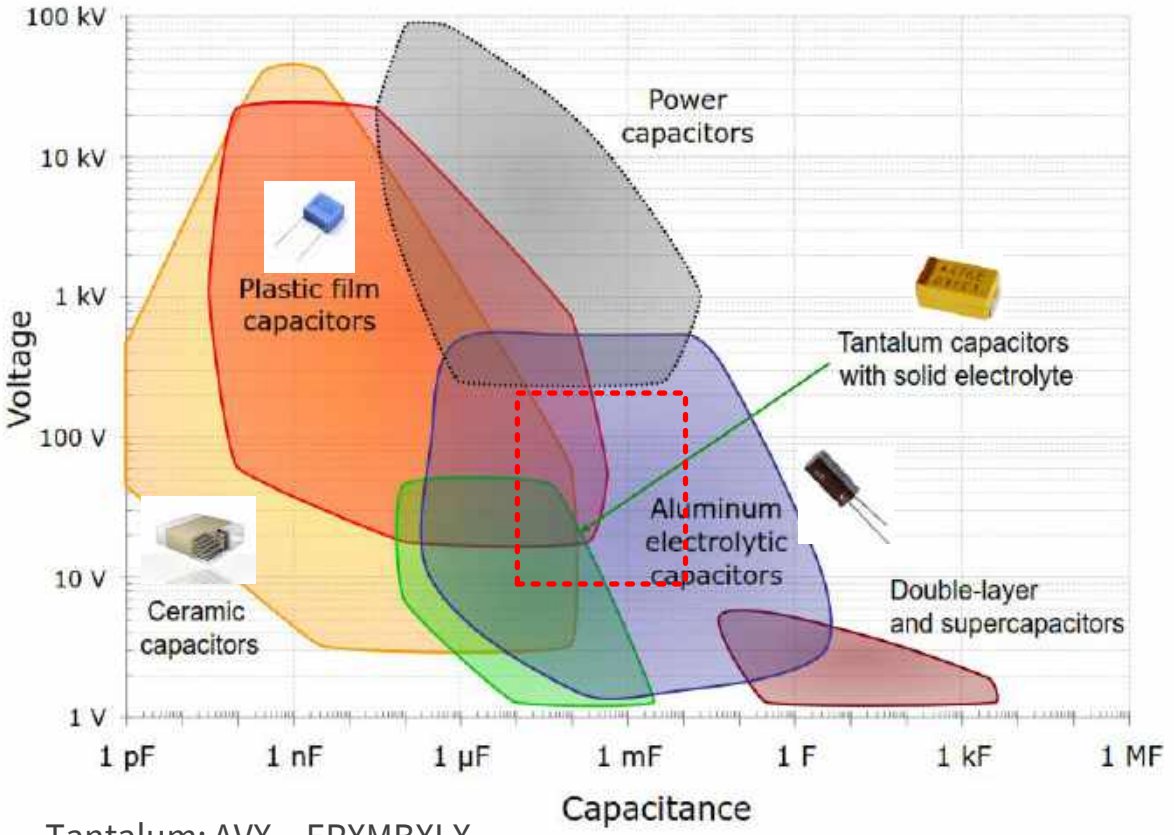


Table 2.3 CAPACITOR SIZING-OPTION COMPARISON

		Tantalum	MLCC	Film	Elec. #1	Elec. #2
Parameter of 1 cap.	C_{unit} $[\mu F]$	10	10	10	10	100
	V_{rating} $[V]$	50	50	50	50	50
	$tan\delta$	0.1	0.1	0.015	0.12	0.12
	$f[kHz]$	10	10	10	10	10
	$ESR_{unit}[m\Omega]$	159	159	23.8	191.1	19.1
	$Volume_{unit}[mm^3]$	118.1	14	1320	43.2	72.2
	Unit price $[KRW]$*	2,390	1,764	3,890	25	60
Parameter of N Cap.	N◇	200	200	200	200	20
	$ESR_{effective}$ $[m\Omega]$	0.8	0.8	0.12	0.96	0.96
	Total volume $[mm^3]$	23,625	2,800	264,000	8,635	1,444.5
	Total cost $[KrW]$	478,000	352,728	77,800	5,000	1,200

*Unit price is referred from Eleparts in October 2022.

◇ N is the number of parallel capacitors.

Tantalum: AVX - EPXMBXLX

MLCC: AVX – EPXUMLVN

Film: WIMA - EPXLX77Y

Electrolytic: EPXKTC4K (10uF) & EPXKTD3G (100uF)

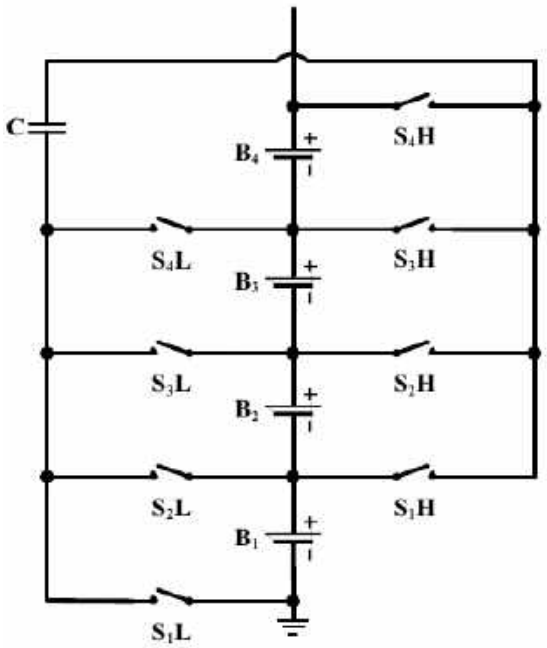
$$ESR = \frac{tan\delta}{\omega C}.$$

$$N = \frac{C_{target}}{C_{unit}}.$$

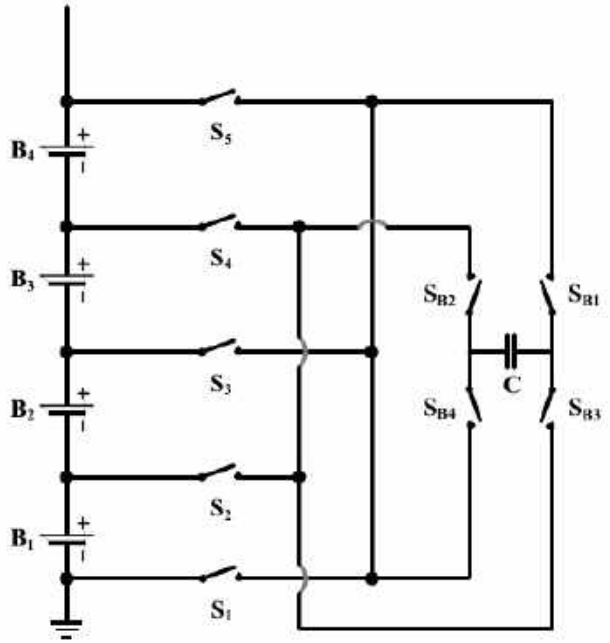
$$Z_{effective} = \frac{Z}{N} = \frac{ESR}{N} - \frac{j}{2N\pi fC},$$

$$ESR_{effective} = real(Z_{effective}) = \frac{ESR}{N}.$$

2.3 SMC-E: Design Consideration – Switch Matrix



Multiplexer structure



Odd-Even structure

Table 2.4 SWITCH-MATRIX STRUCTURE COMPARISON

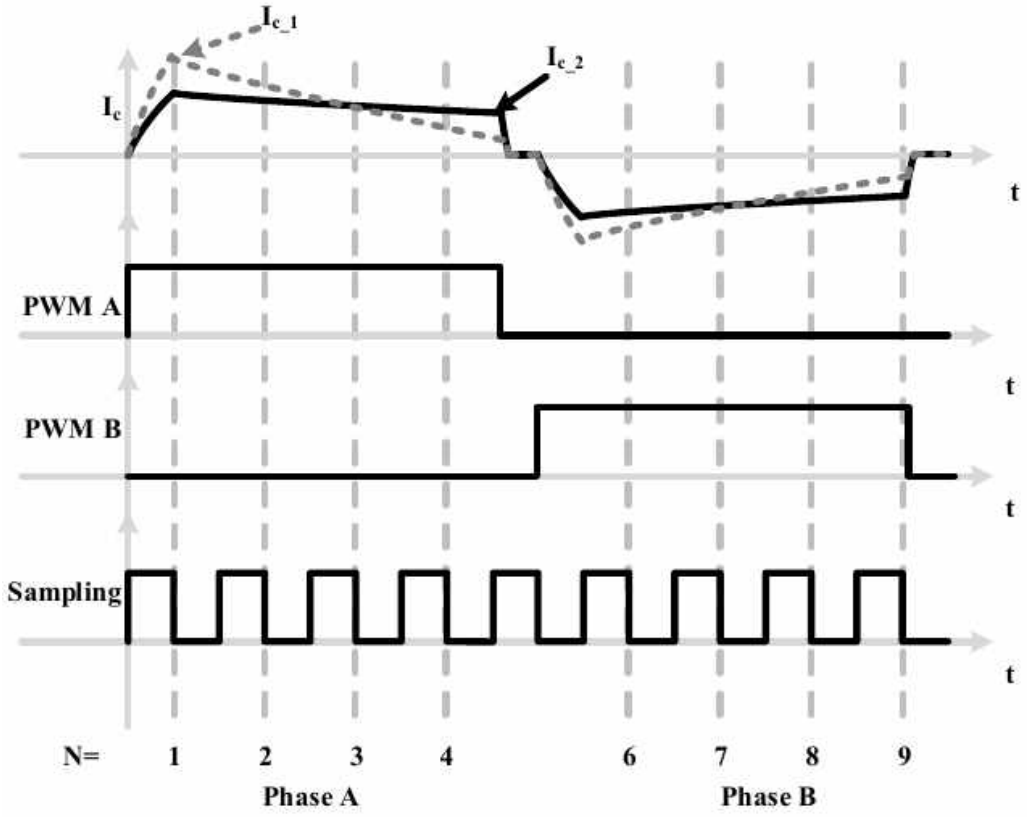
Structure	Number of switches	Number of control signal	Number of activated switches
Multiplexer	2N	N	2
Odd-Even	N+5	N+3	4

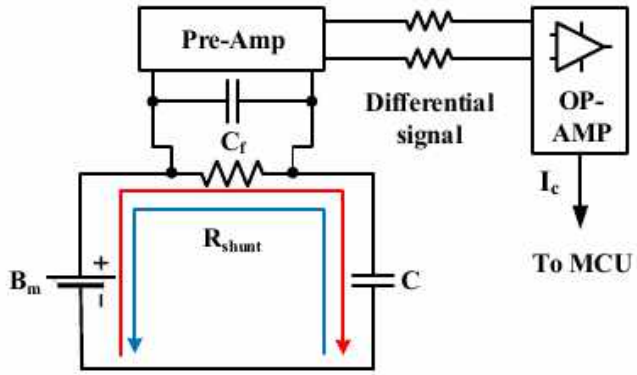
- **Number of switches** in the **odd-even structure** is less than the **multiplexer structure when N > 6.**
- **The odd-even structure** requires **more complex control circuit** than **the multiplexer**.
- During the operation, odd-even structure activates 4 switches simultaneously which increase the resistance of the circuit

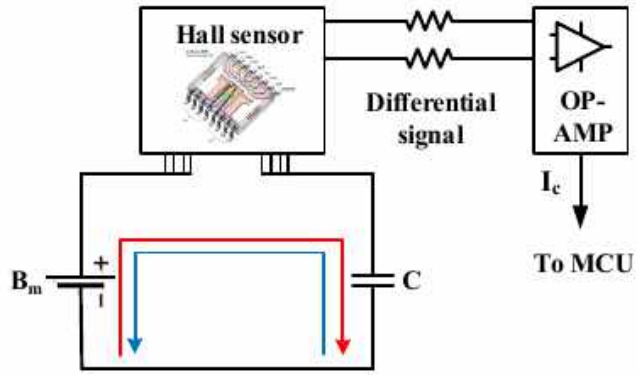
➔ **Reduce the balancing current.**

$$R_{circuit} = RB + N * R_{d\ on} + ESRc + Rother$$

2.3 SMC-E: Design Consideration – Current Sensing Method



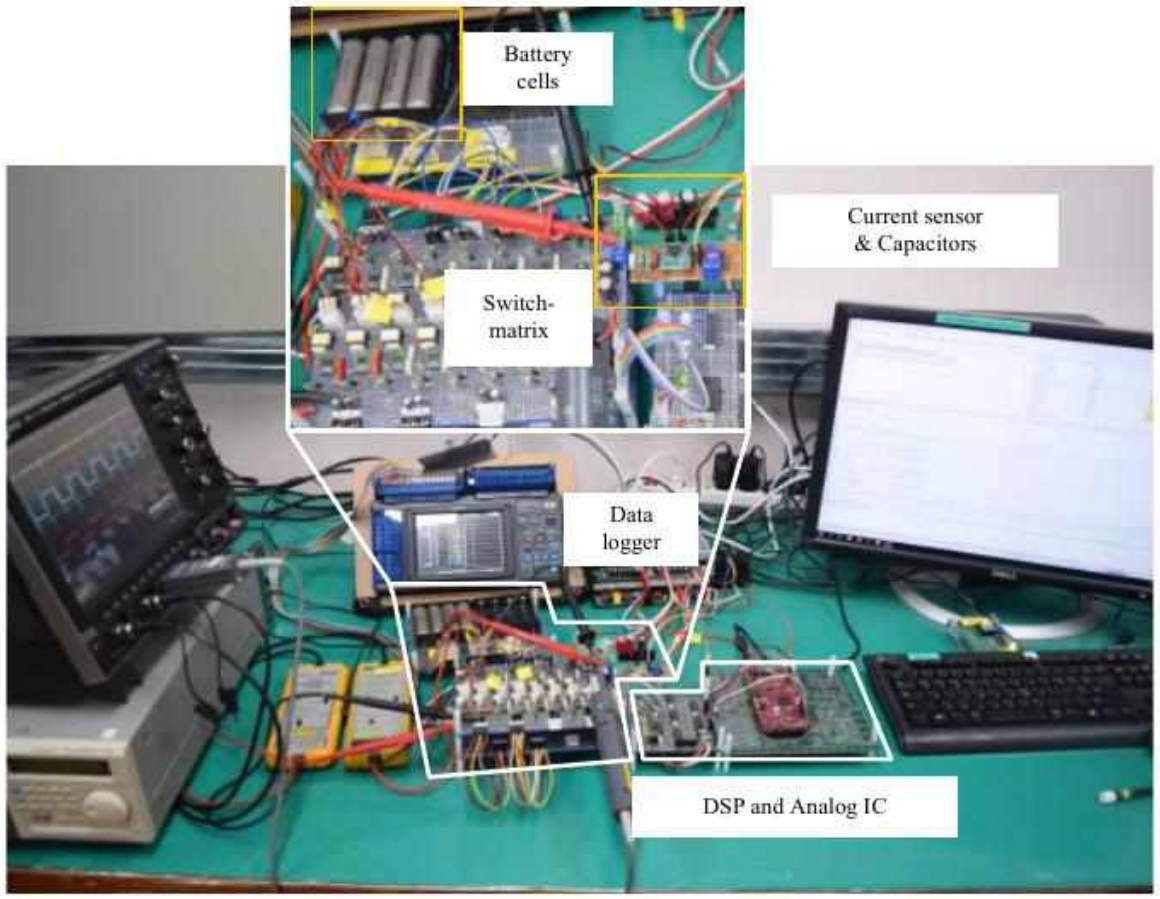




- Since the **current waveforms of the different cell-pairs** are **heterogeneous**, balancing current is **measured at multiple point to calculate the average value**.
- **Hall effect current sensor** has a lower bandwidth than the **shunt resistor,** but **don't increase the resistance of the circuit.**

$$R_{circuit} = RB + N * R_{d\ on} + ESRc + Rother$$

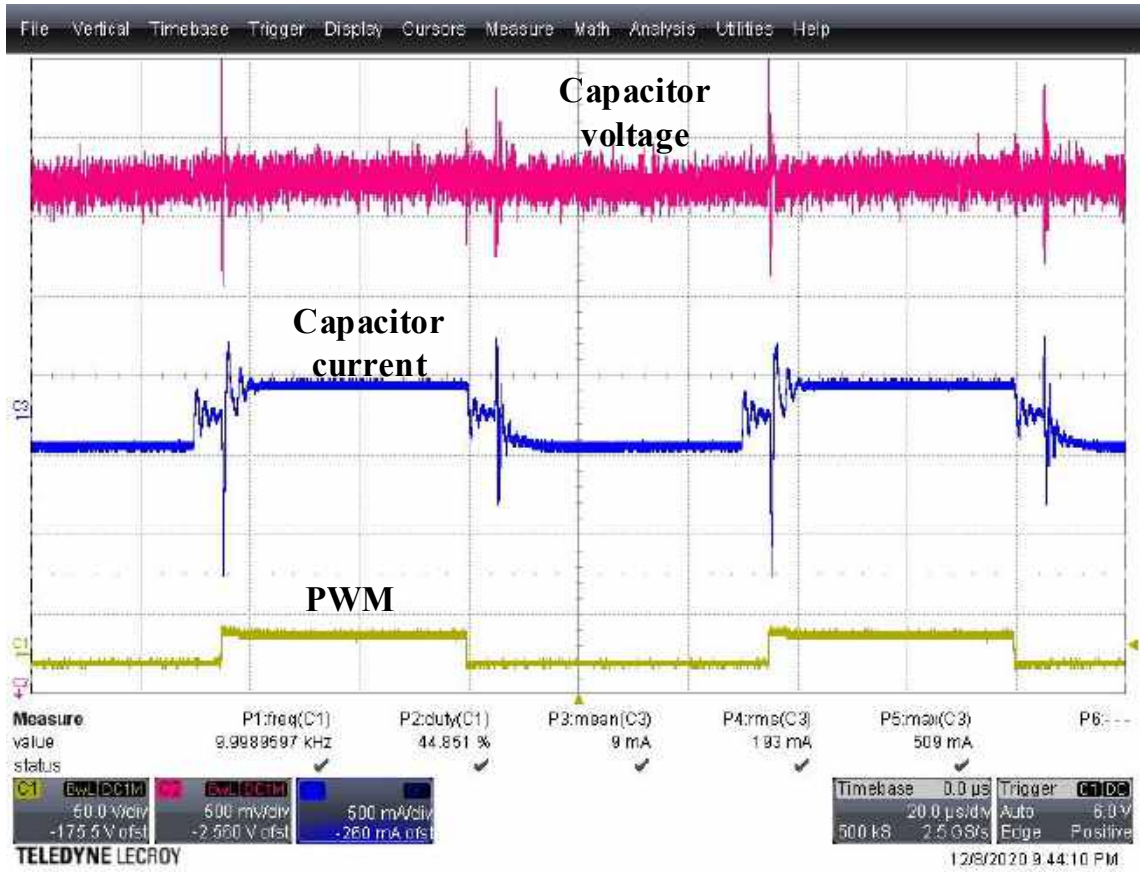
2.4 SMC-E: Performance Verification – Design Assessment

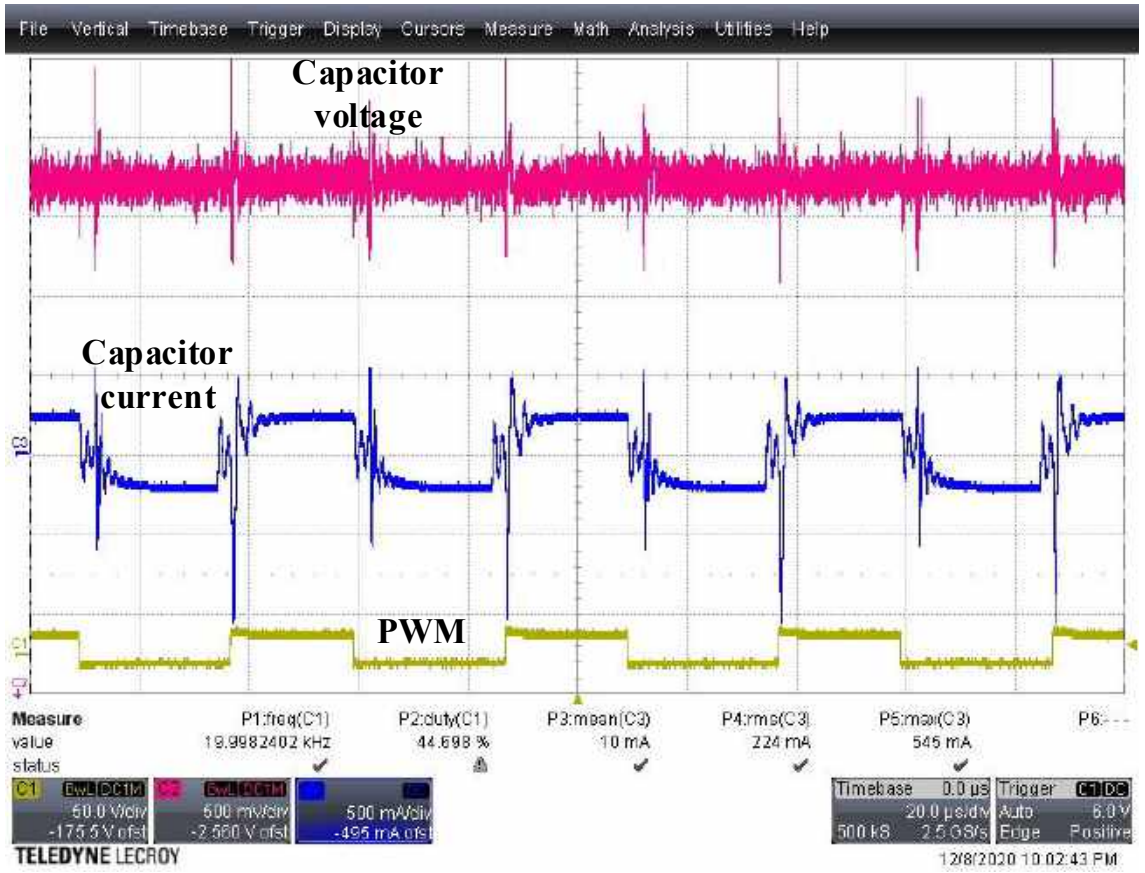


- Balancing current of two cells (V_{B1} = 4.163V; V_{B2}=3.843V) is compared to verify the theoretical calculation.
- $R_{circuit}$ = 0.45Ω
- Based on the theoretical analysis, four design options are assessed:
  - **Design #1:** 1000uF/10kHz → I = 193mA
  - **Design #2:** 2000uF/10kHz → I = 206mA
  - **Design #3:** 2000uF/10kHz → I = 212mA
  - **Design #4:** 4000uF/20kHz → I = 224mA

*Difference between the designs are small due to the high resistance of the circuit.

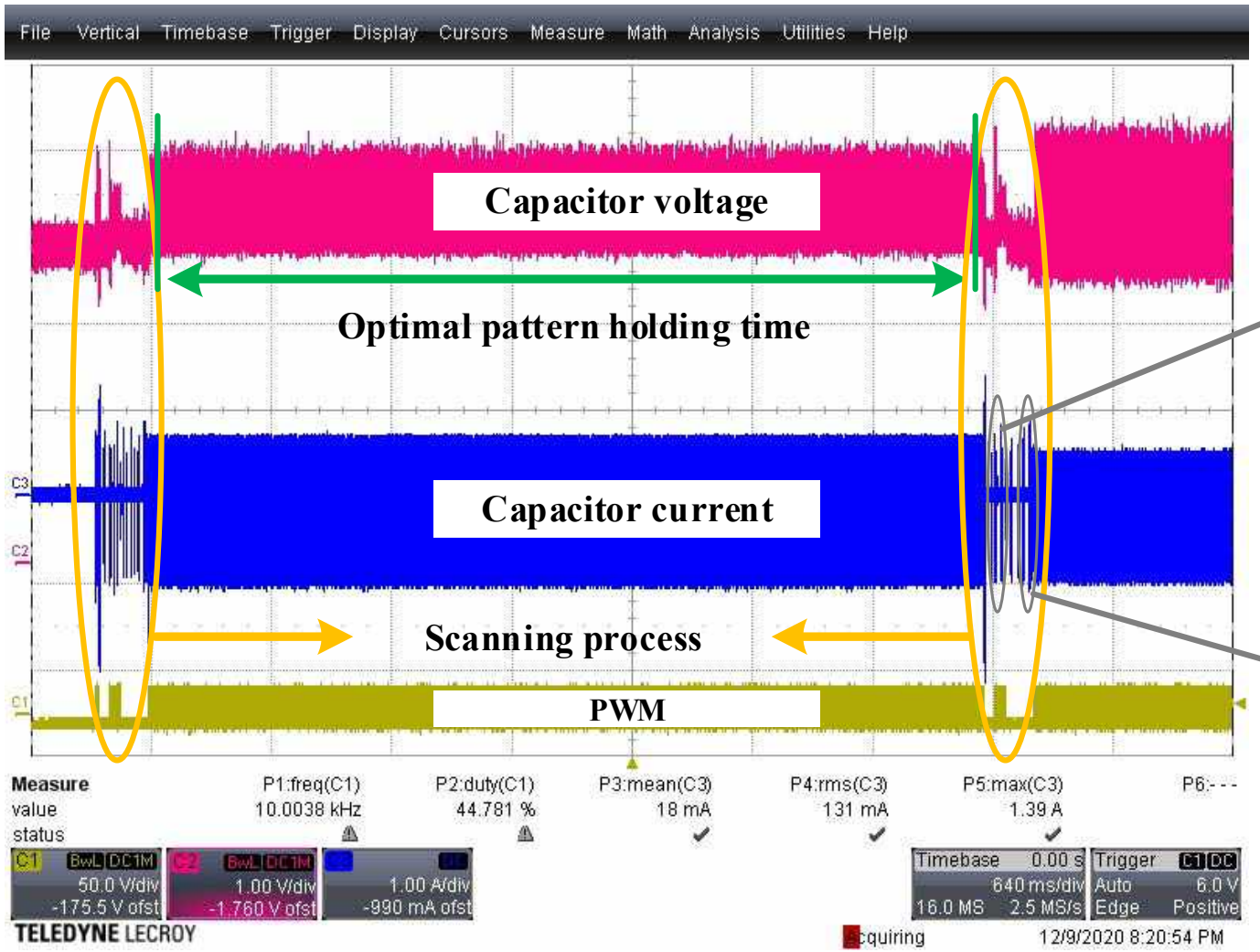
2.4 SMC-E: Performance Verification – Design Assessment

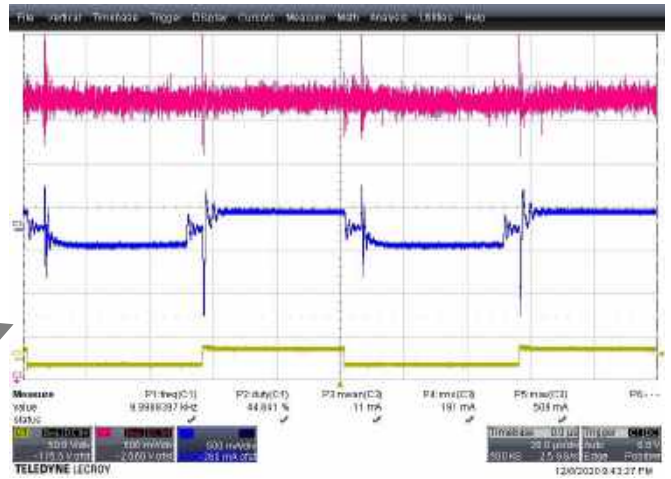


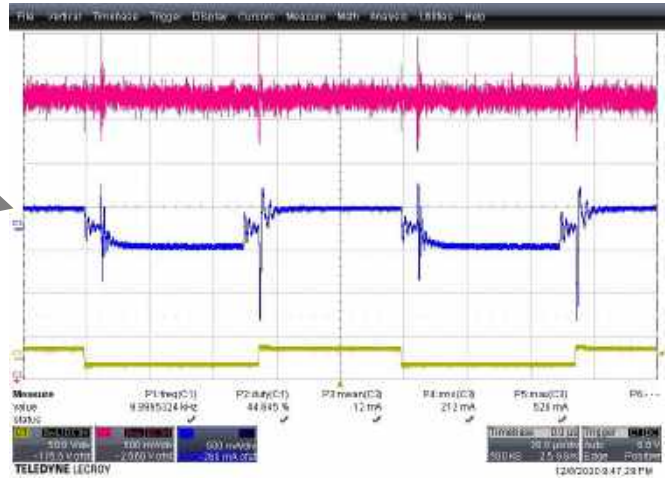


*__Resistance of the circuit__ should be redesigned **instead of increase the balancing capacitance and switching frequency.**

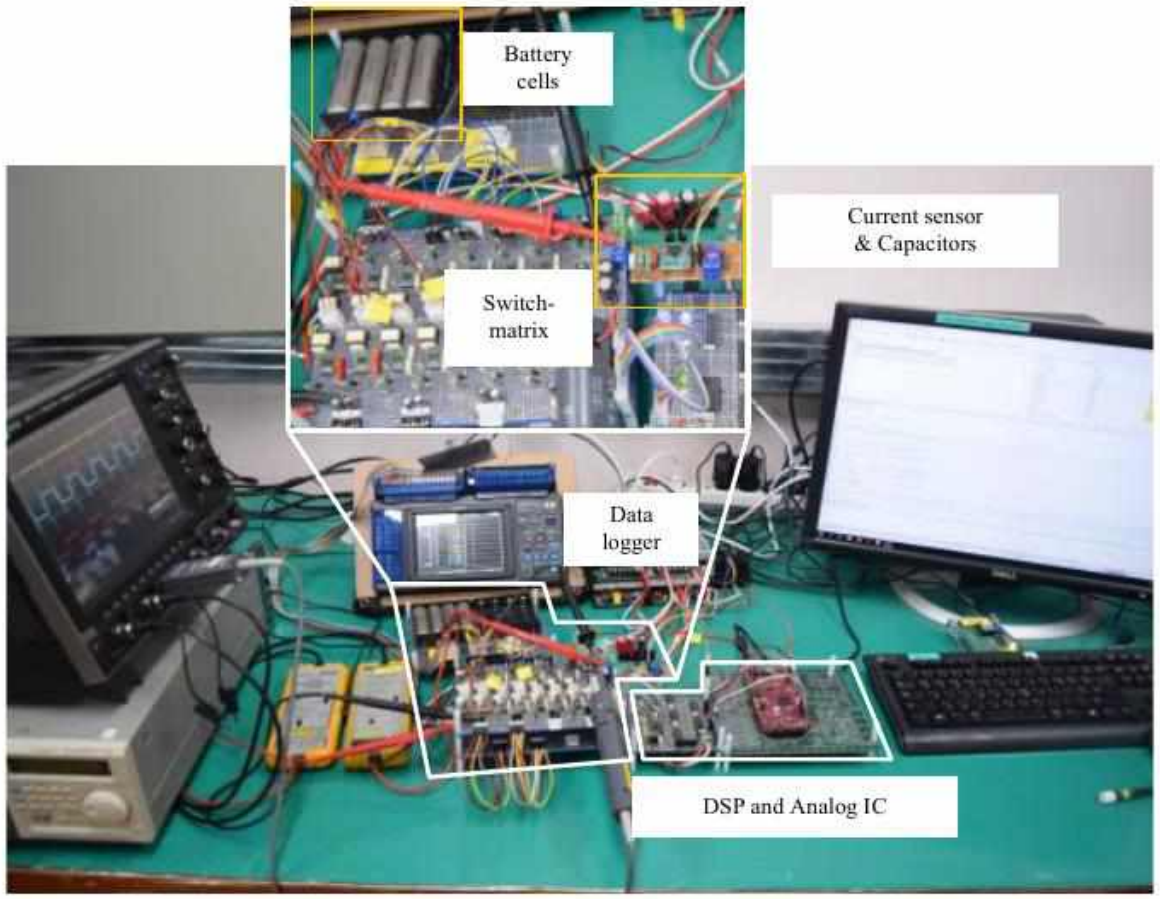
2.4 SMC-E: Performance Verification – Optimal Pairing Algorithm







2.4 SMC-E: Performance Verification – Experiments Setup



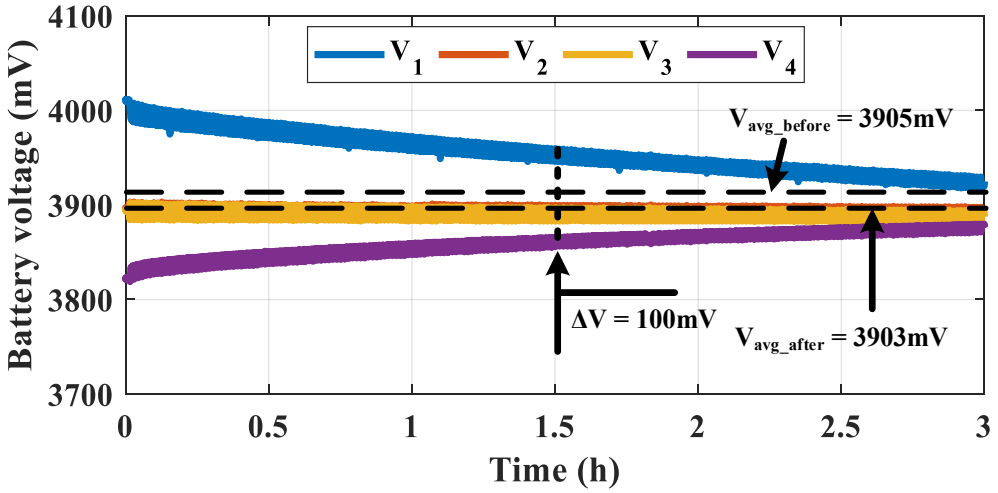
Parameter	Setting
C (uF)	2000
f_{sw} (kHz)	10
Cell	LG 18650HD2 - 3.65V/2600mAh
t_cutoff (h)	3 for cases #1 and #2; 4h for case #3

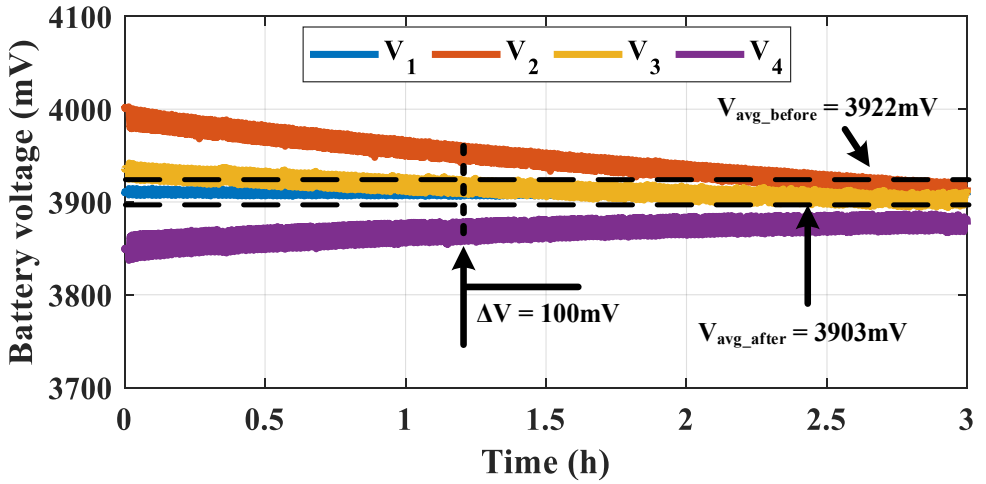
- **Battery voltages** are **recorded by a data logger** (Hioki LR8402-20) during the equalizing process.
- **Equalization process is stopped after 3h** for the performance assessment.
- Recorded data is **plotted by Matlab for a visualization**.
- SMC-E is **tested under three different cases** with **different initial voltage distribution**.

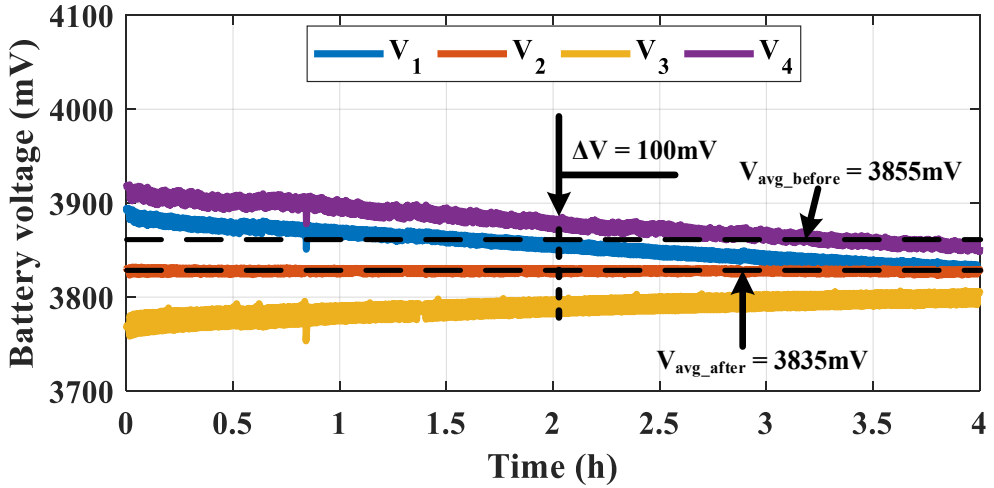
2.4 SMC-E: Performance Verification – Equalization

Table 2.6 EXPERIMENTAL RESULTS-BATTERY VOLTAGES (mV)

	Cell #1	Cell #2	Cell #3	Cell #4	V_{avg}	ΔV
Initial #1	4000	3900	3910	3820	3905	180
Exp. #1	3920	3900	3900	3895	3903.75	25
Initial #2	3900	4010	3940	3840	3922.5	170
Exp. #2	3910	3910	3905	3890	3903.75	20
Initial #3	3900	3830	3760	3930	3855	170
Exp. #3	3840	3840	3800	3850	3835	40







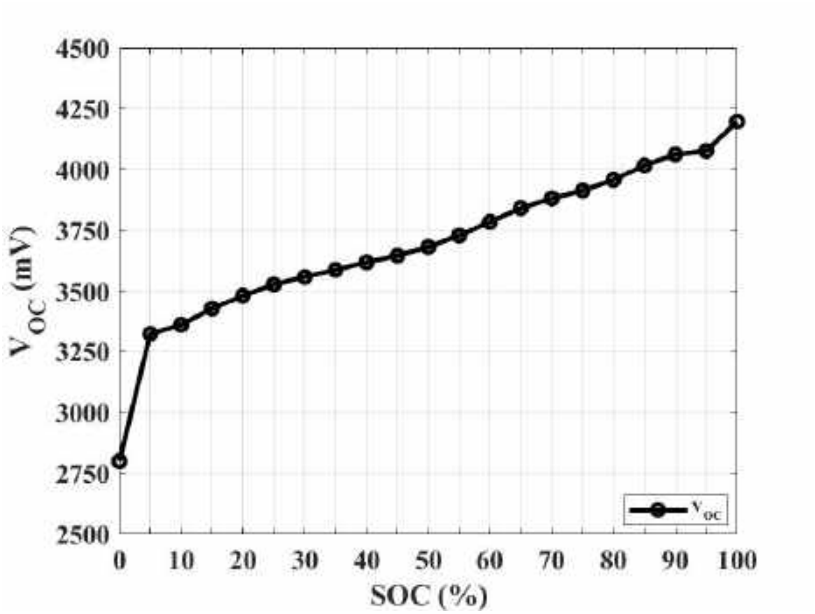
2.5 Conclusion of the Chapter

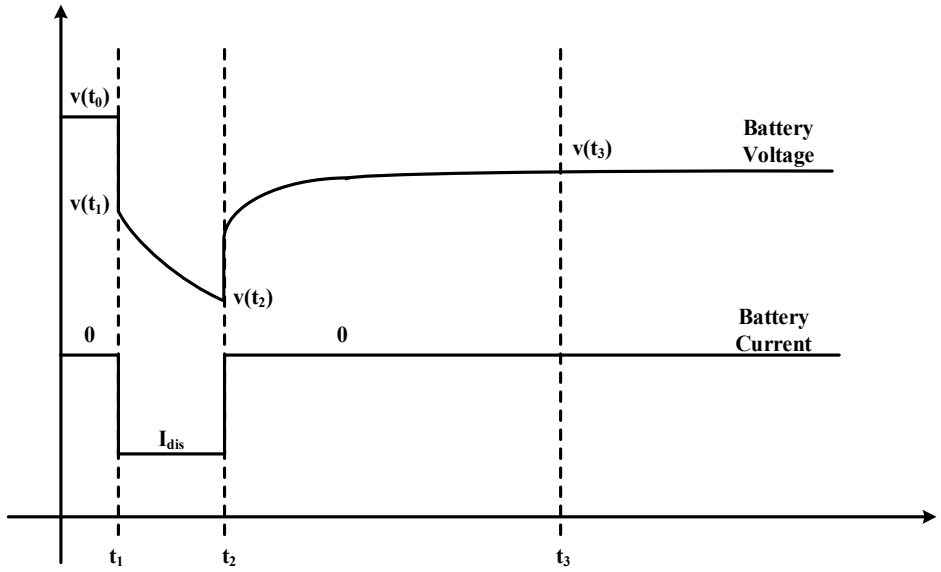
- **A step-by-step development and design of the SMC-E** to mitigate the cell-inconsistency is introduced.
- **Theoretical analysis** are provided in order to **design the balancing capacitance and switching frequency for the SMC-E**.
- **Design consideration** for the **switch-matrix structure, gate driving method, and current sensing scheme** is provided.
- **Optimal pairing algorithm** show an effectiveness performance to overcome the impact of the initial distribution scenarios.
- **Hardware experimental results** verified the **equalization capability and the theoretical operation principle of the SMC-E.**

Agenda

1. Introduction and Research Motivation
2. Switch-Matrix Capacitor Equalizer for the Cell level
3. Novel Simulation Techniques for Performance Assessment of SET-E in Long-term Operation
   - 3.1 Real Time Simulation
   - 3.2 Unified Average Model Based Simulation
   - 3.3 Conclusion of the Chapter
4. Module Equalizer System for Series and Parallel Connected Battery Modules
5. Conclusions and Future Works

3.1 Real Time Simulation

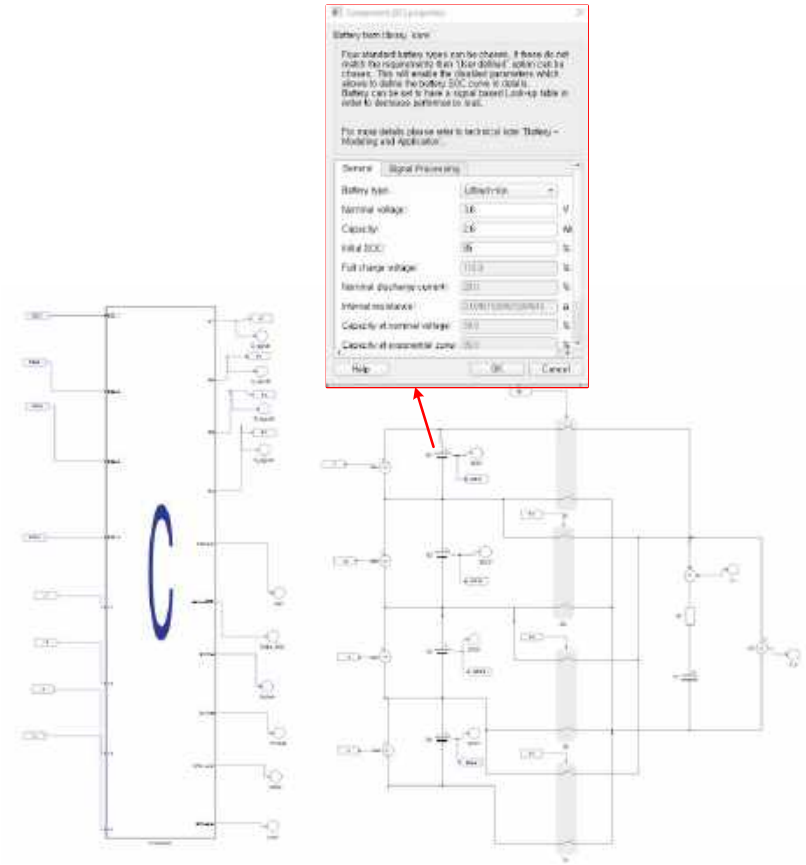


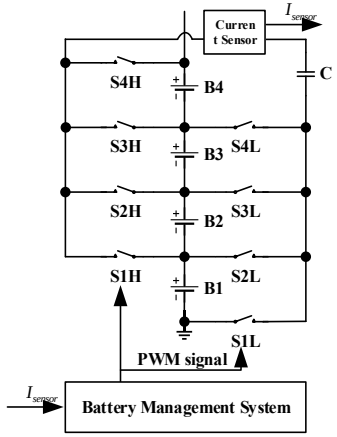


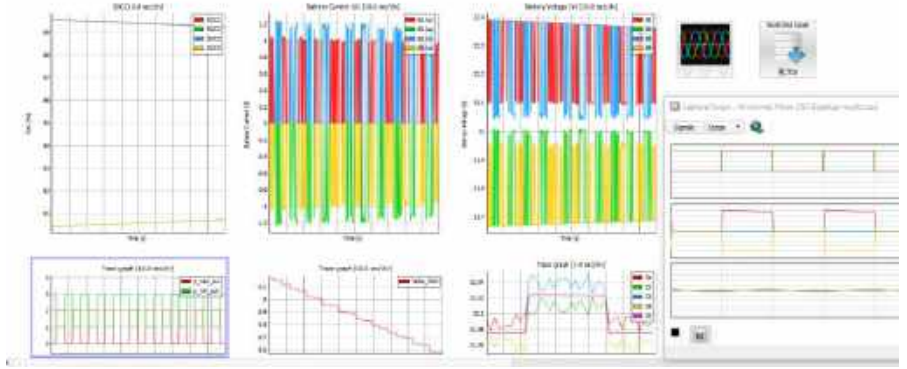
- To have **a fair performance comparison** for various equalizers, the tests **must be occurred under the same conditions**.
- Since **energy level of the cell cannot be directly measured**, **it is difficult to set a similar initial conditions for the cells in every tests**.
- **Polarization effect** of the battery also **affect the fairness of the comparison**.

➔ Simulations should be used.

3.1 Real Time Simulation – Description







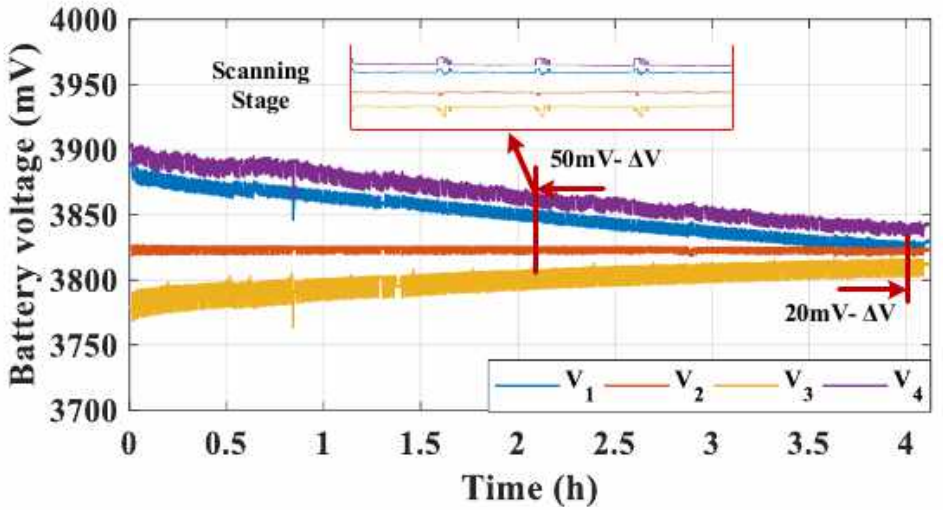
*Various test scenarios can be set for the performance comparison.

3.1 Real Time Simulation – Accuracy Comparison with Hardware

Page 70 in Thesis

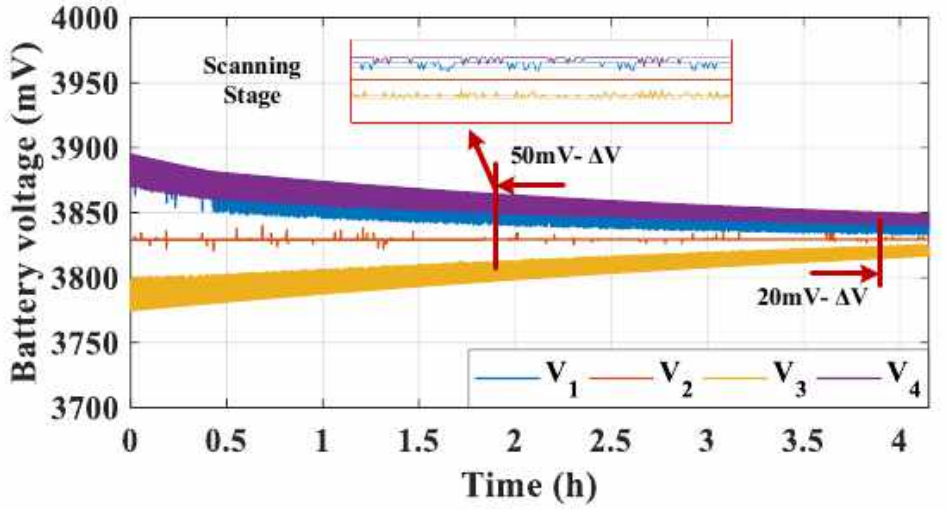
Parameter	Setting
C (uF)	2000
f_{sw} (kHz)	10
Cell	LG 18650HD2 - 3.65V/2600mAh
t_cutoff (h)	4

Hardware experimental results

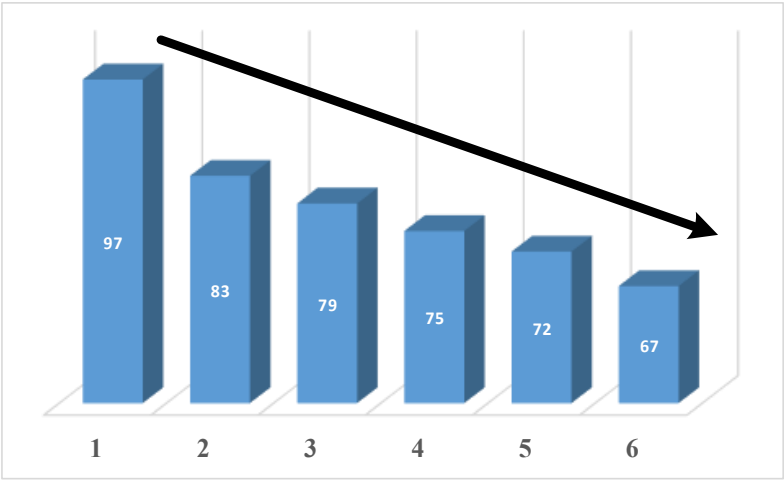


	#1	#2	#3	#4	ΔV
Initial	3898	3825	3760	3912	152
Exp.	3823	3823	3814	3844	20
HIL 4 cells	3826	3823	3820	3839	19

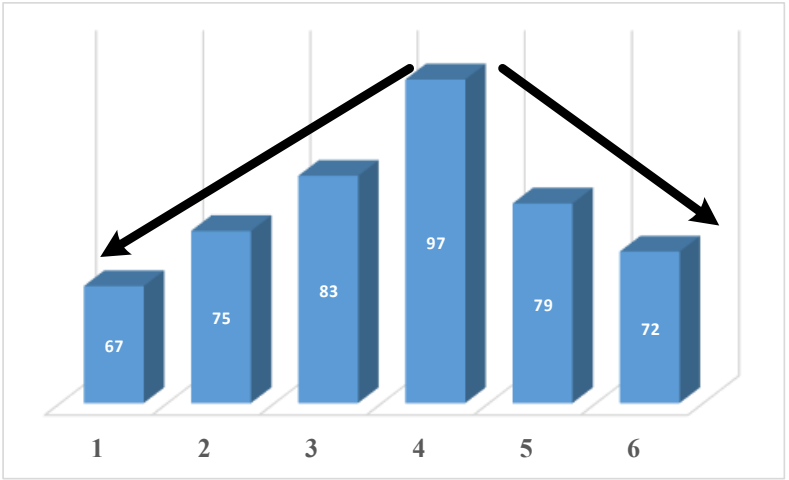
RTSS results



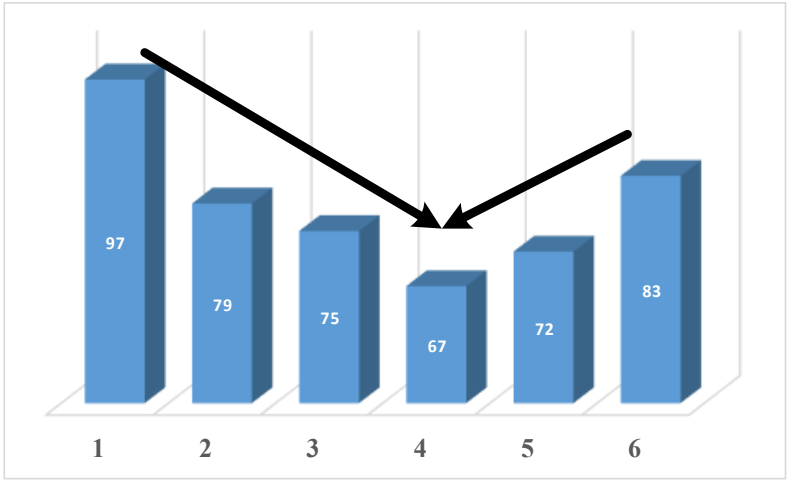
3.1 Real Time Simulation – Equalization Performance Assessment



Descending Order



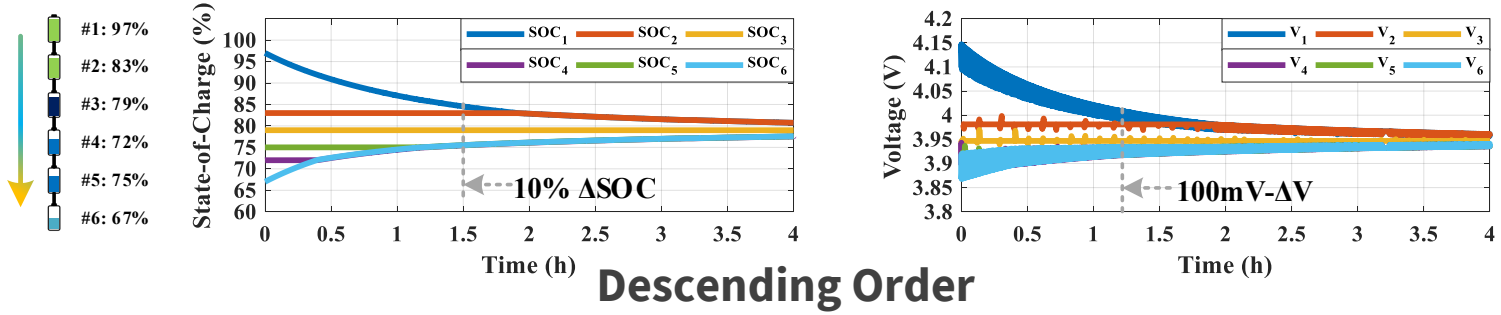
Convex Order



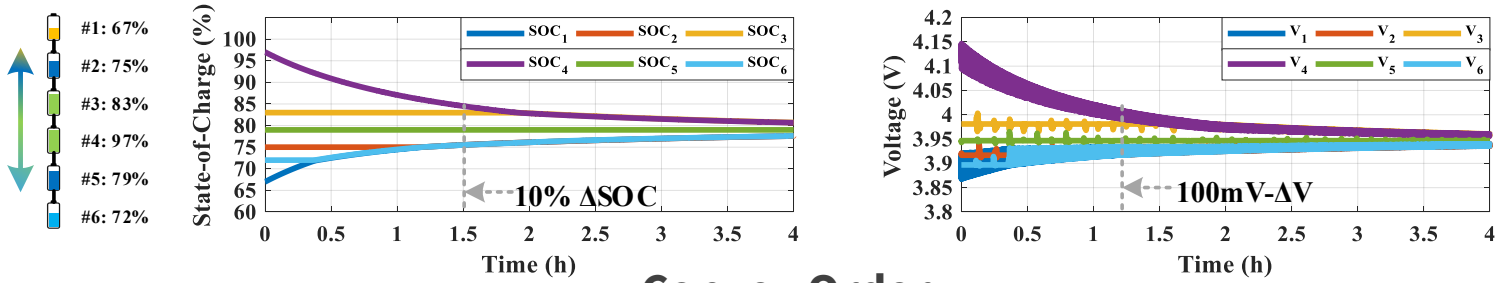
Concave Order

- SMC-E is implemented **for 6S1P battery string** to assess the **impact of the cell number** on the equalization performance.
- Same design of SMC-E is tested under **three different scenarios**.
- Through the tests, the **performance dependency on the initial condition** of SMC-E is assessed.

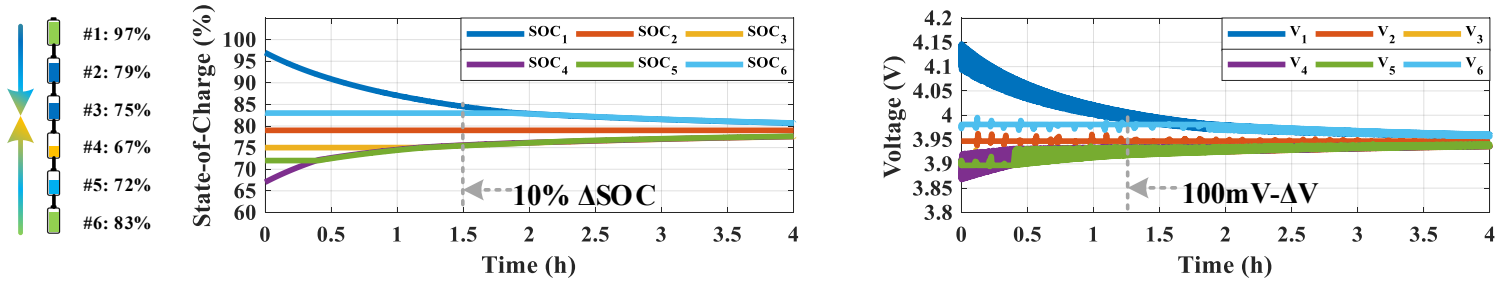
3.1 Real Time Simulation – Equalization Performance Assessment



Descending Order



Convex Order



Concave Order

- Voltage and SOC profiles of the SMC-E are similar in all scenarios.
- SMC-E can effectively mitigates the cell-inconsistency under different initial distribution of the cells.
- Influence of the cell number on the performance of the SMC-E exists but it is weak.

3.1 Real Time Simulation – Equalization Performance Assessment

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Table 3.2 SUMMARY OF PERFORMANCE INDICES

	$DoSE[\%]$	$DoVE[\%]$	$SR_{SOC}[\%/h]$	$SR_V[mV/h]$	*Charge transfer scheme*	*Additional sensing*	*Initial voltage distribution dependency*
SMC-E	$89 \sim 90.6$	$92.3 \sim 93$	$17.3 \sim 18.1$	$154.7 \sim 178$	**Direct 1-to-1**	**One current sensor**	**Weak**

$$DoSE = \frac{\Delta SOC_{initial} - \Delta SOC_{final}}{\Delta SOC_{initial}}$$

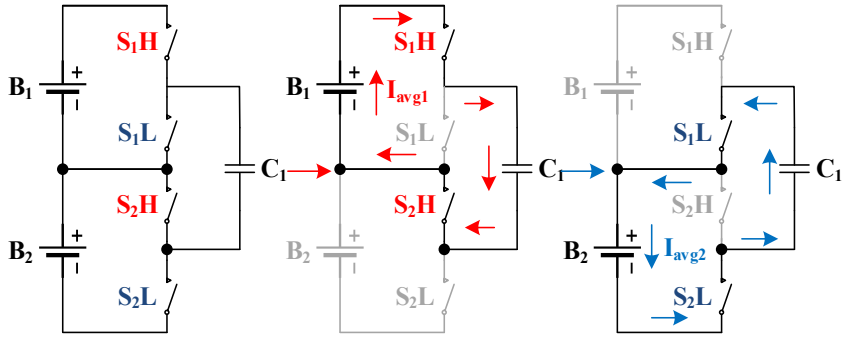
$$SR_V = \frac{\Delta V_{init} - \Delta V_t}{t_{process}}$$

$$DoVE = \frac{\Delta V_{initial} - \Delta V_{final}}{\Delta V_{initial}}$$

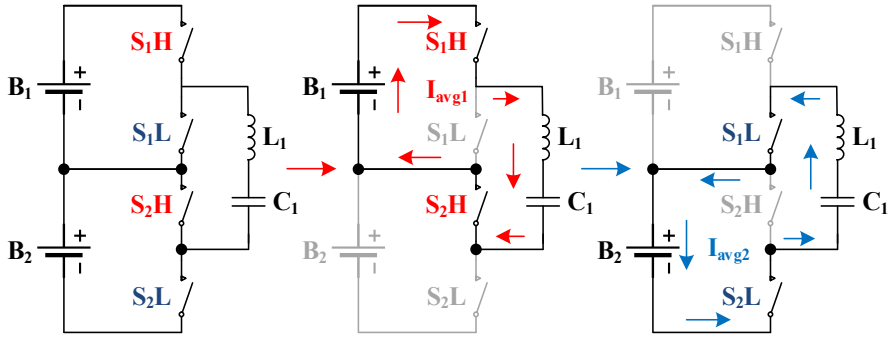
$$SR_{SOC} = \frac{\Delta SOC_{init} - \Delta SOC_t}{t_{process}}$$

- **Various data can be recorded** during the equalization process by RTSS to **assess more evaluation criteria** than **by the hardware experiments**.
- **Performance indices of the SMC-E** are high in all test scenarios.

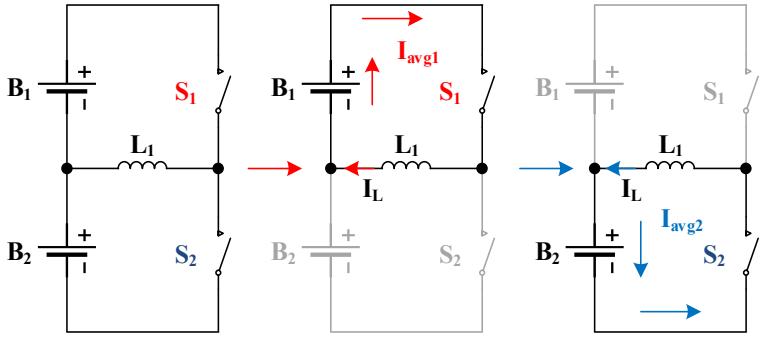
3.2 Unified Average Model Based Simulation



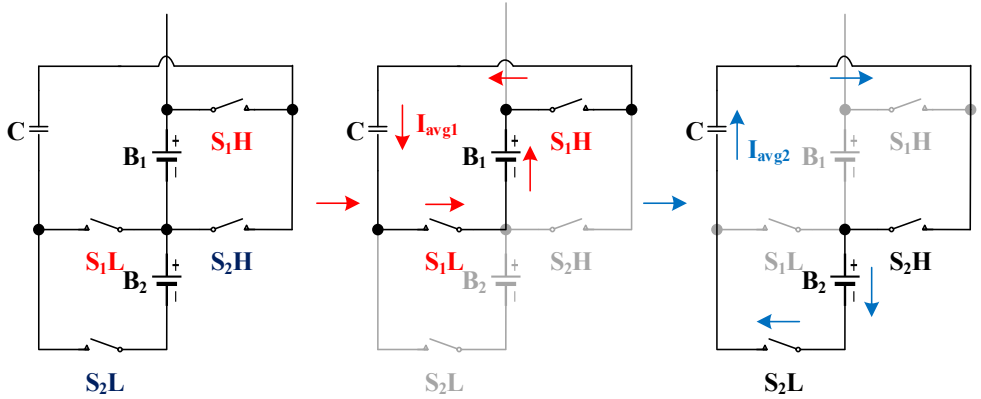
Switched Capacitor Equalizer



Switched Resonance Equalizer



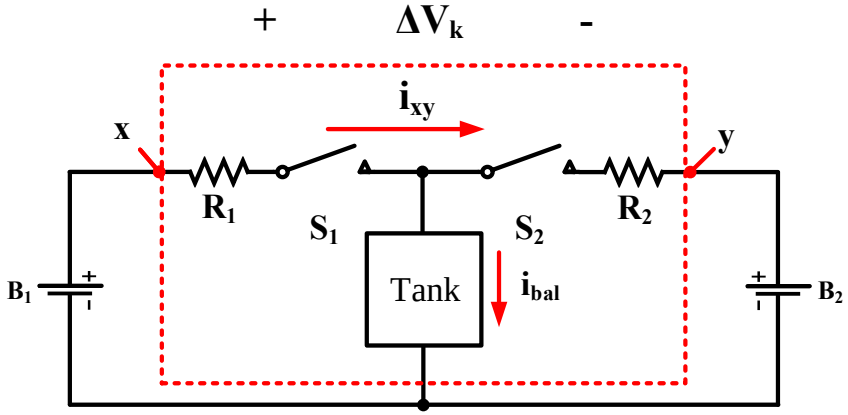
Switched Inductor Equalizer



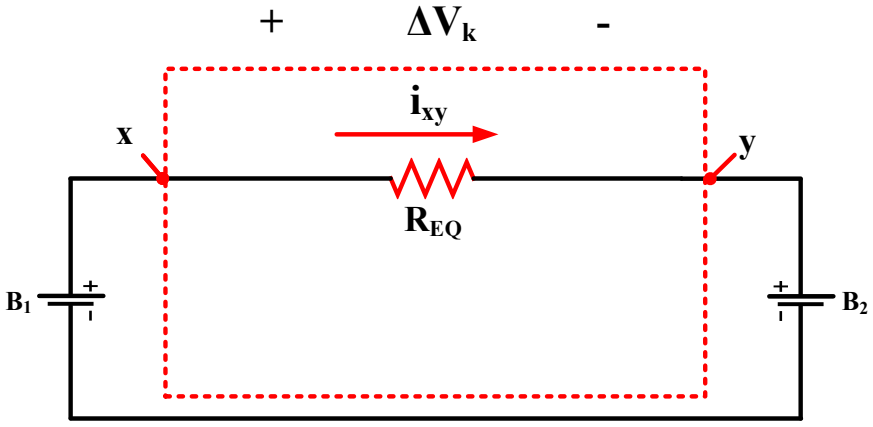
Switch Matrix Capacitor Equalizer

➢ **SC-E, SR-E, SI-E, and SMC-E** have **a similar operation principle** that can be grouped into one group.

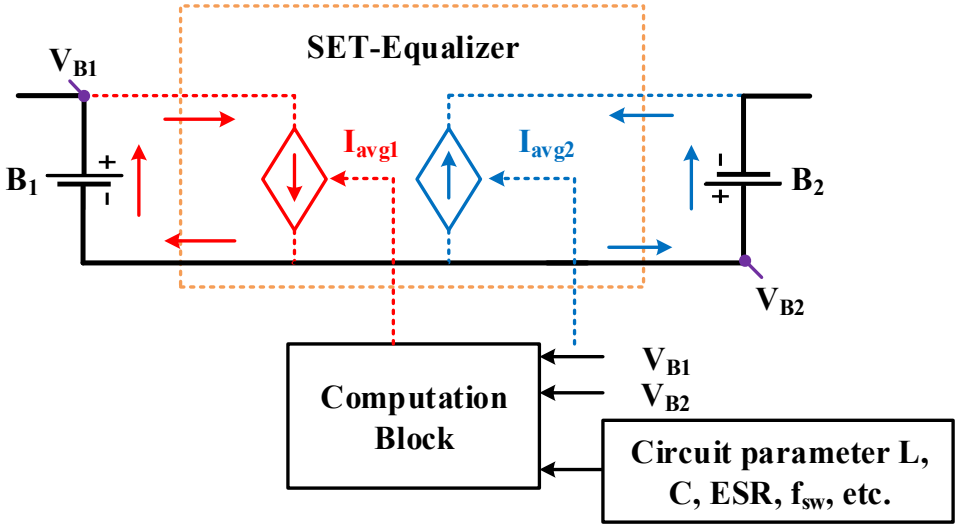
3.2 Unified Average Model Based Simulation



Equivalent Circuit of SET-E



R_{EQ} model



Unified Average Model

- **Switching model** is replaced by **an average model** to **reduce the sampling rate, and thus, decrease the runtime**.
- **Main idea of UA-model** is to identify the **average amount of charge that flows into or out the cells** during the equalization process.

3.2 Unified Average Model Based Simulation

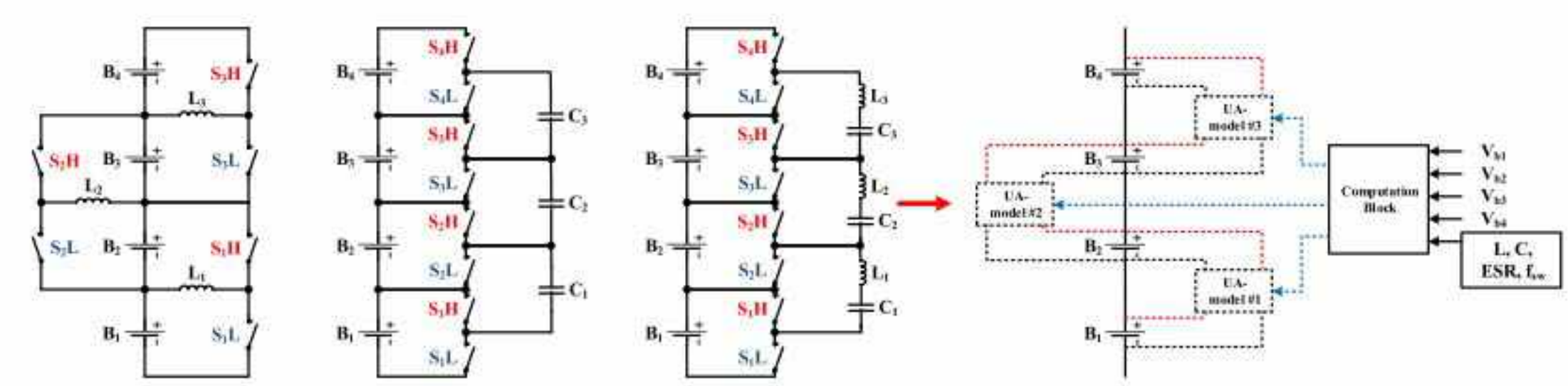
Table 3.3 AVERAGED EQUALIZATION CURRENT CALCULATION FOR UA-MODEL

Topology	Key formula
SC-E & SMC-E	$I_{avg1} = \frac{1}{2} C f_{sw} (V_{B1} - V_{B2}) \left(1 - exp(\frac{-D_1}{f_{sw} R_1 C})\right)$ $I_{avg2} = \frac{1}{2} C f_{sw} (V_{B2} - V_{B1}) \left(1 - exp(\frac{-D_2}{f_{sw} R_2 C})\right) exp(\frac{-1}{2 f_{sw} R_2 C})$
SR-E	$I_{avg1} = \frac{1}{2} C f_{sw} (V_{B1} - V_{B2}) \left(1 + exp(\frac{-\beta_1 \pi}{\omega_{r1}})\right)$ $I_{avg2} = \frac{1}{2} C f_{sw} (V_{B2} - V_{B1}) \left(1 + exp(\frac{-\beta_2 \pi}{\omega_{r2}})\right)$
SI-E	$I_L = \frac{D V_{b1} - (1-D) V_{b2}}{D^2 (R_1 + R_L) + (1-D)^2 (R_2 + R_L)}$ $I_{avg1} = D I_L$ $I_{avg2} = -(1-D) I_L$

- Based on the **theoretical analysis** of the equalizer, the **key formula for UA-model** is obtained.
- **Circuit parameters** are set for UA-model based on the **design of equalizer**.
- **Cell voltages** are **measured to calculate the average balancing current** of the cells at **each cycle of the equalizer**.

➔ **Balancing current changes** as the **voltage deviation decreases**.

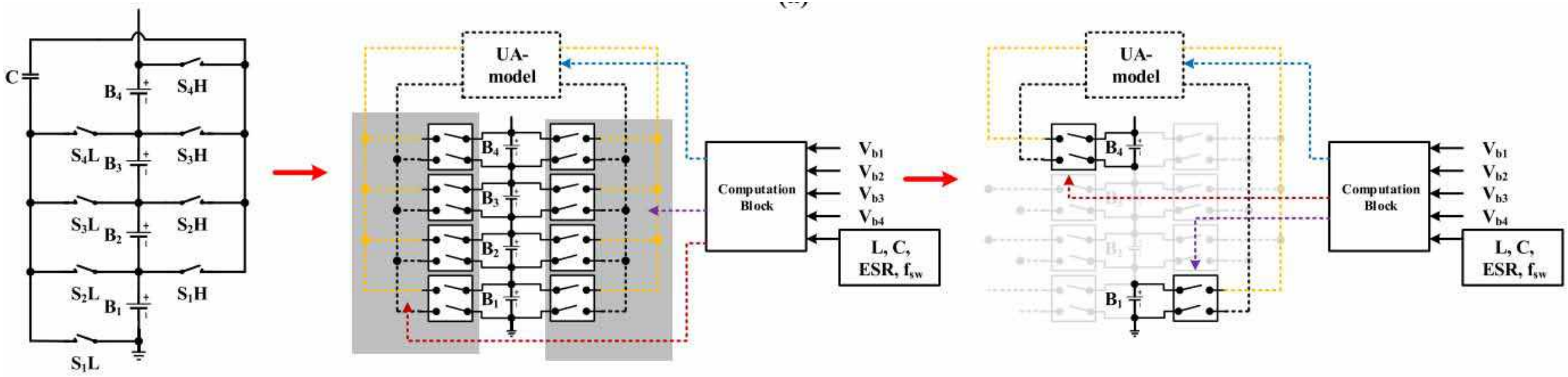
3.2 Unified Average Model Based Simulation - Implementation



- **Topology configuration** decide **the number of UA-model in the simulation.**
- **Conventional single-tier SI-E, SC-E, and SR-E** utilize **multiple equalizers** to transfer energy between the cells.

➔ **Multiple UA-models** are used to **emulate the equalization process**.

3.2 Unified Average Model Based Simulation - Implementation



- **SMC-E** only use **one capacitor** to transfer energy between the cells.
- **Only one UA-model** is required in the simulation.
- **A contactor network** is added to choose the cell pair.

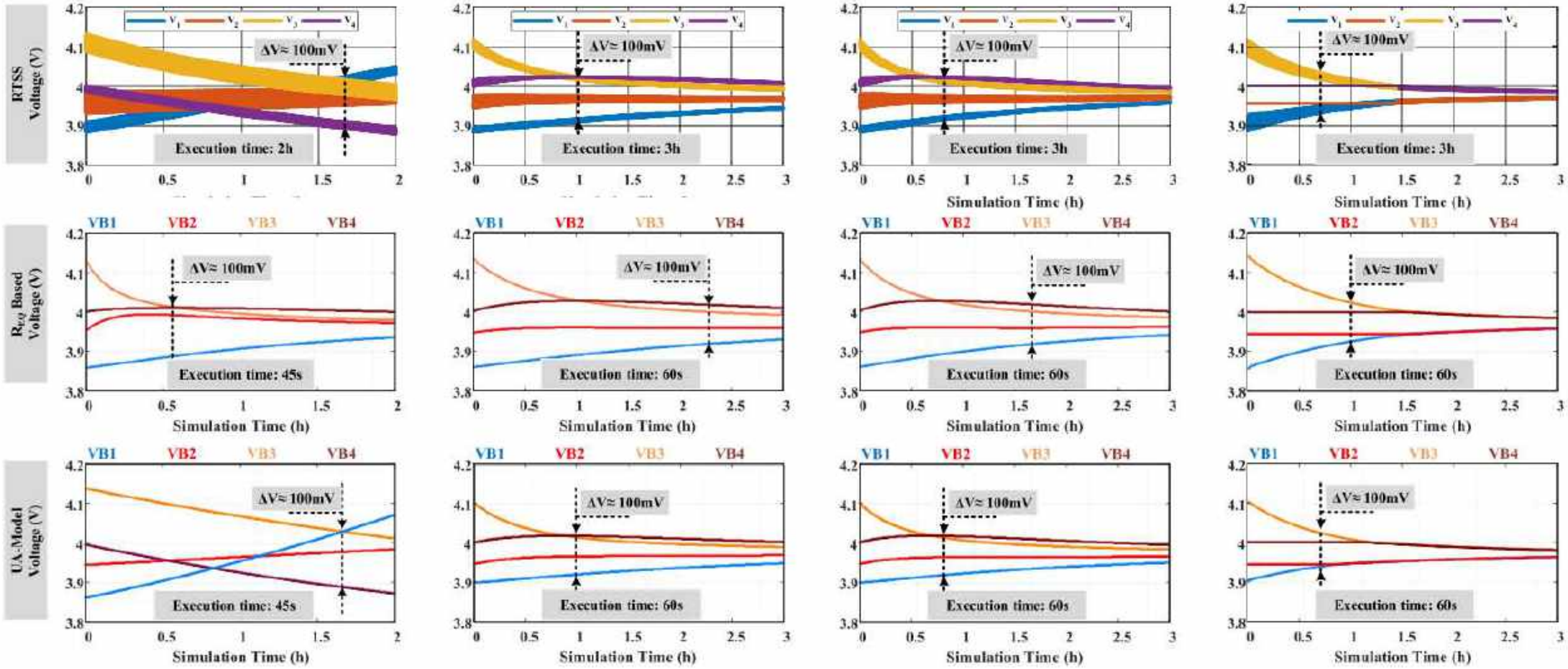
3.2 UA-Model Based Simulation – Accuracy Comparison with RTSS

Table 3.4 CIRCUIT PARAMETER SETTING

Topology	SI-E	SC-E	SR-E	SMSC-E
Circuitry Parameters	$f_{sw} = 20\ kHz$ $L = 400\ \mu H$ $R = 0.15\ \Omega$ $D = 0.45$	$f_{sw} = 20\ kHz$ $C = 2200\ \mu F$ $R = 0.15\ \Omega$ $D = 0.45$	$f_{sw} = 15\ kHz$ $C = 200\ \mu F$ $L = 0.47\ \mu H$ $R = 0.15\ \Omega$ $D = 0.45$	$f_{sw} = 20\ kHz$ $C = 2200\ \mu F$ $R = 0.15\ \Omega$ $D = 0.45$
Initial SOC	$SOC_{1,\ 2,\ 3,\ 4} = 70,\ 80,\ 95,\ 85\ [\%]$			

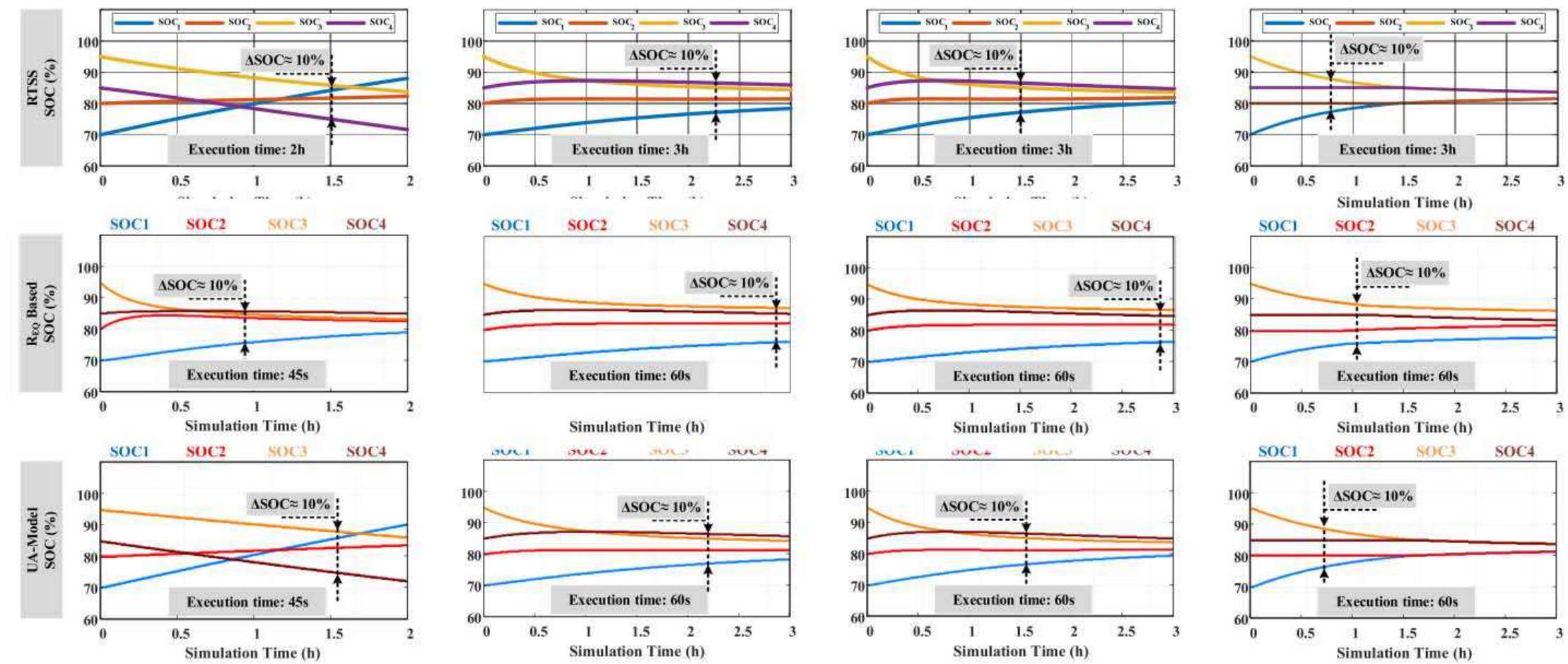
- **UA-model** is implemented for a **4S1P cell string**.
- **The operating profiles of the cells** such as **voltage, SOC, and current** of the equalization process through the **UA model** are compared with the results through the **RTSS and REQ model**.

3.2 UA-Model Based Simulation – Accuracy Comparison with RTSS



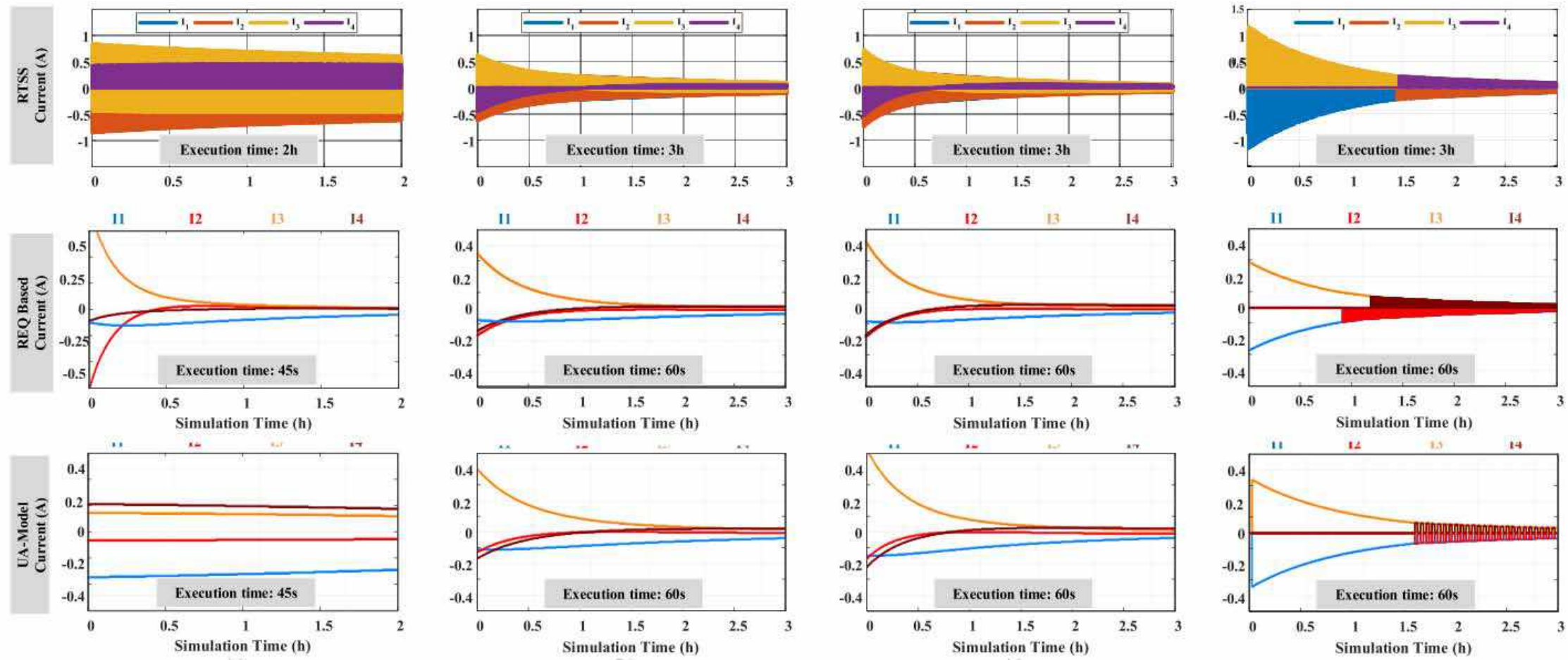
SI-E SC-E SR-E SMC-E

3.2 UA-Model Based Simulation – Accuracy Comparison with RTSS



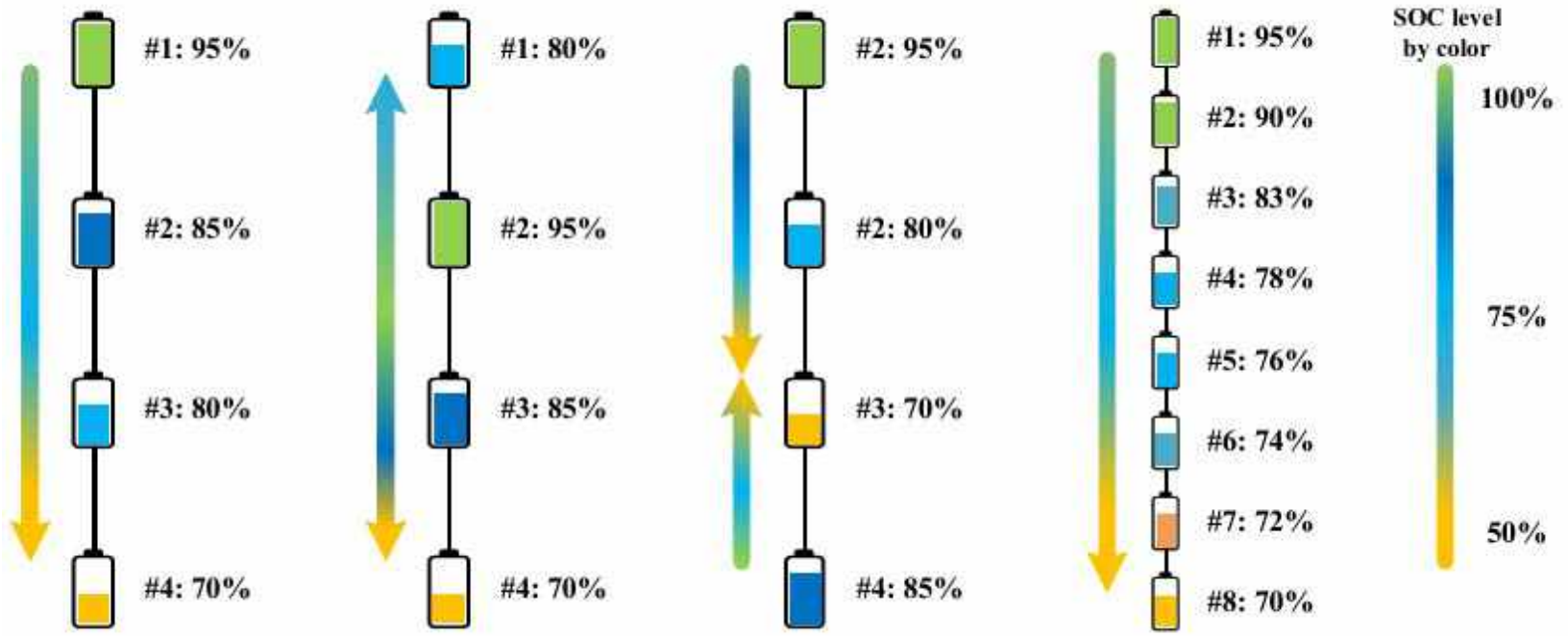
SI-E SC-E SR-E SMC-E

3.2 UA-Model Based Simulation – Accuracy Comparison with RTSS



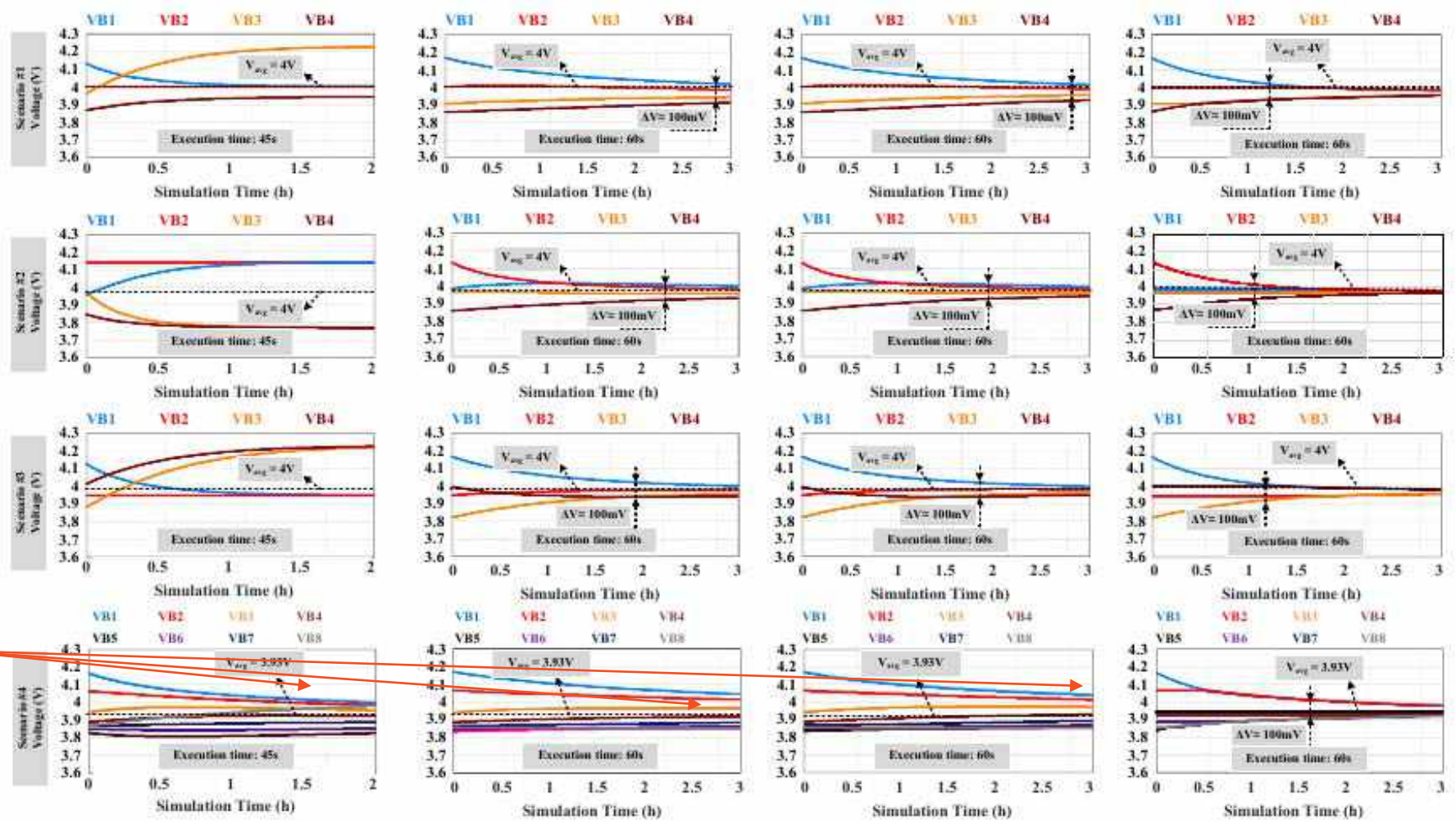
SI-E SC-E SR-E SMC-E

3.2 UA-Model Based Simulation – Performance Assessment



- **Same tests with the RTSS** are applied for **UA-model to verify its merits**.

3.2 UA-Model Based Simulation – Performance Assessment

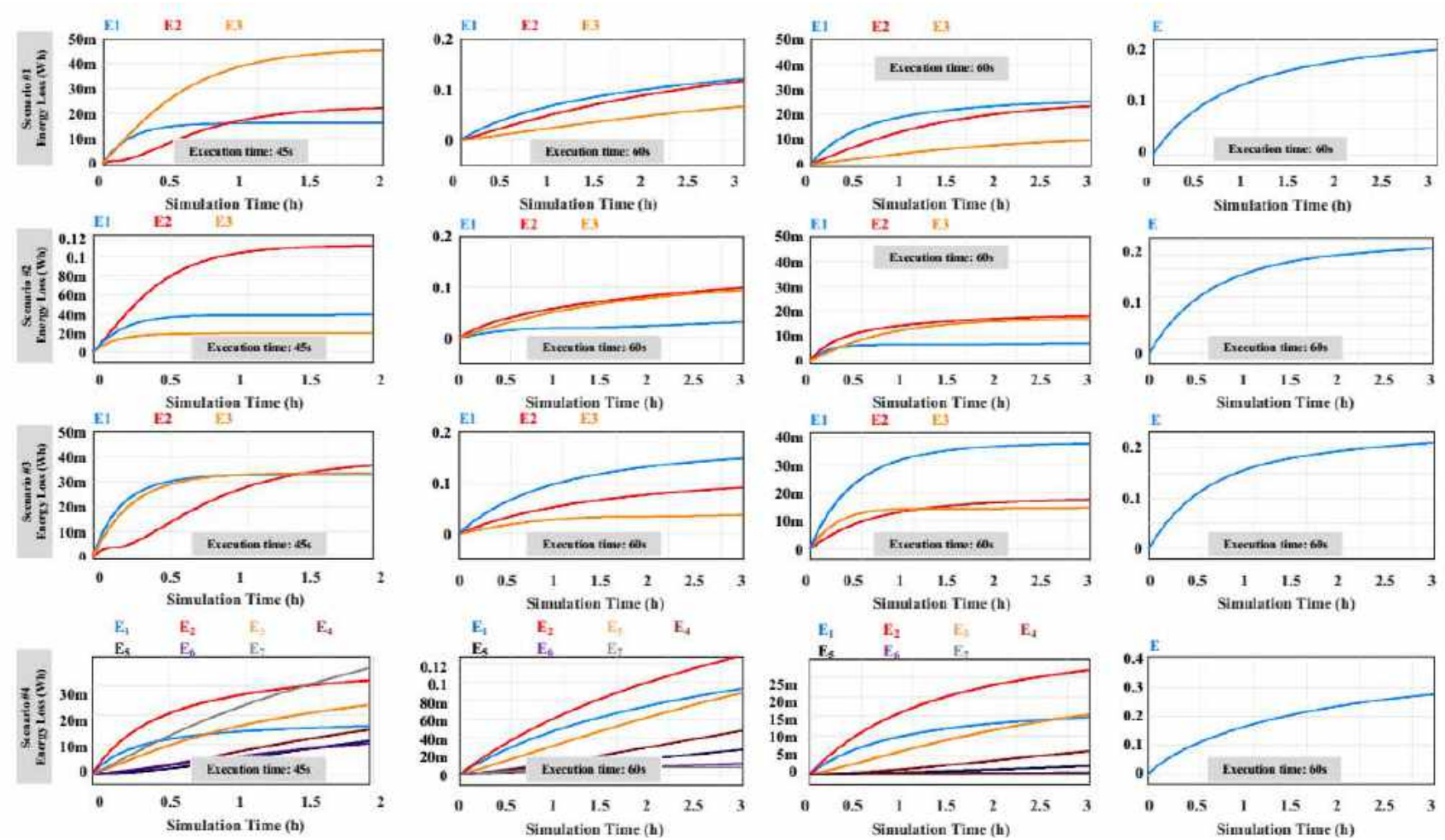


SI-E SC-E SR-E SMC-E

Performance is reduced.

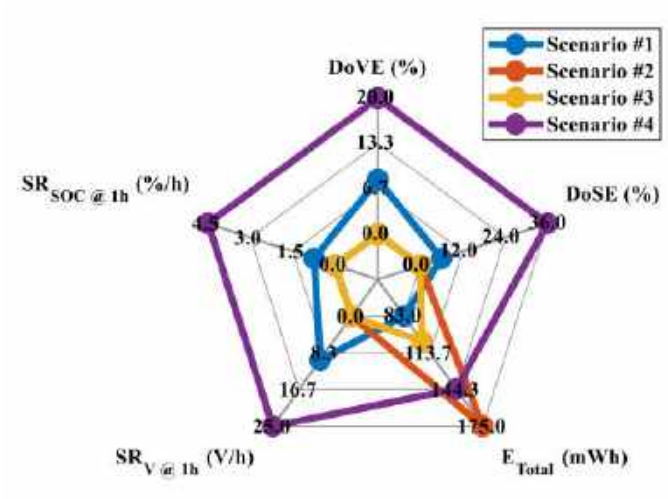
Influence of the cell number exists, but it is less than that of the other equalizers.

3.2 UA-Model Based Simulation – Performance Assessment

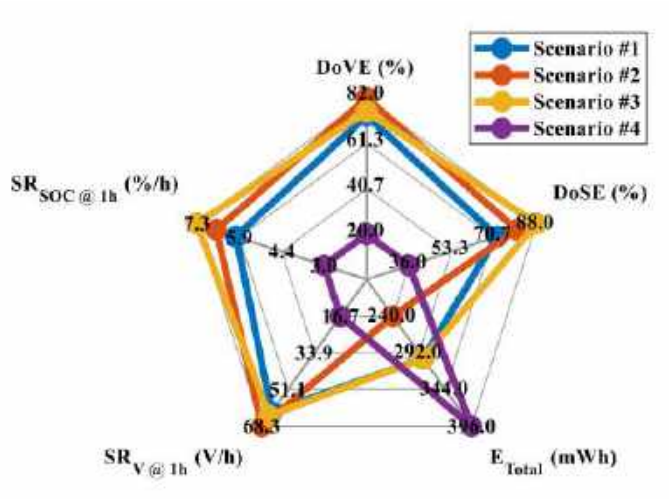


3.2 UA-Model Based Simulation – Performance Assessment

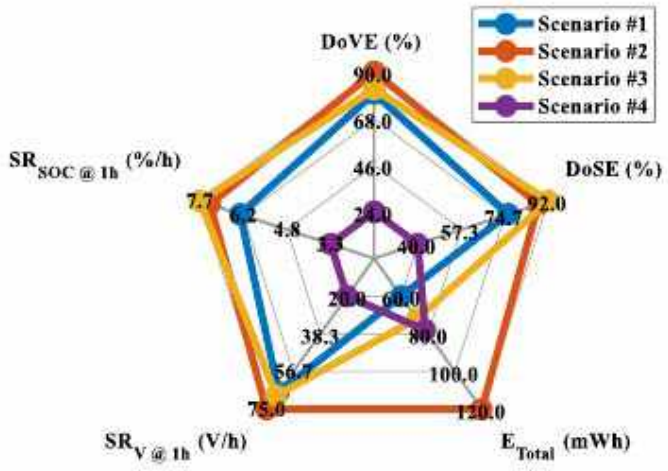
SI-E



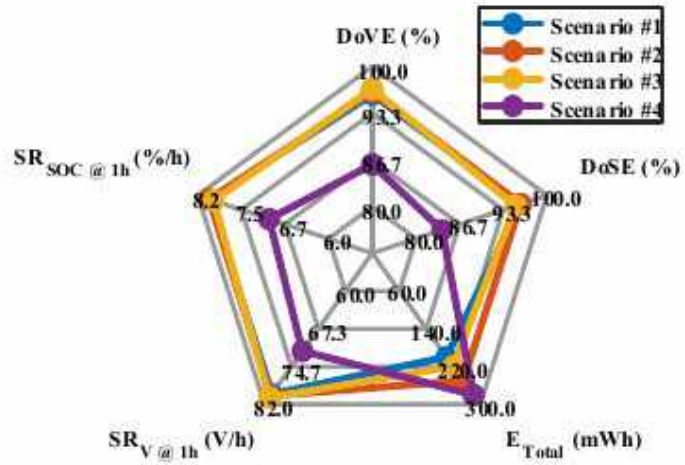
SC-E



SR-E



SMC-E



3.3 Conclusion of the Chapter

- Two simulation methods are introduced in order to assess and compare the performance of various equalizers.
- Real time simulation is a powerful evaluation platform in terms of accuracy, but its execution time is long and the number of component is limited.
- UA-model can emulate hours equalization process just in a short time without any limitation of component number.
- Both real time simulation and UA-model based simulation can be used to verify the various designs of the equalizer.
- To save time, it is recommended to use the UA model for baseline testing and design considerations prior to real-time simulation testing and hardware experiments.

Agenda

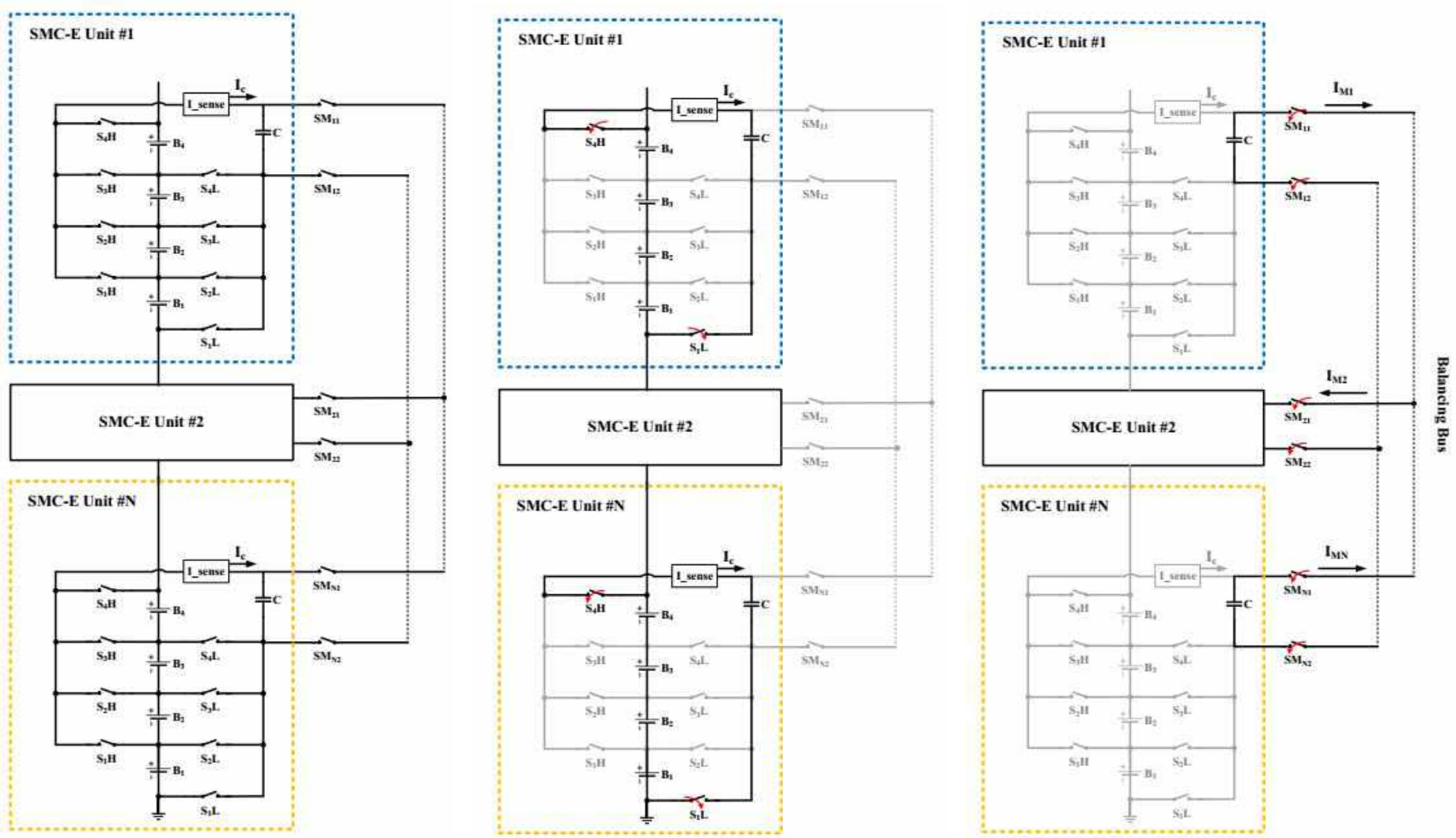
1. Introduction and Research Motivation
2. Switch-Matrix Capacitor Equalizer for the Cell level
3. Novel Simulation Techniques for Performance Assessment of SET-E in Long-term Operation
4. Module Equalizer System for Series and Parallel Connected Battery Modules

   4.1 Extended Version of SMC-E for Series-connected Modules

   4.2 Extended Version of SMC-E for Parallel-connected Modules

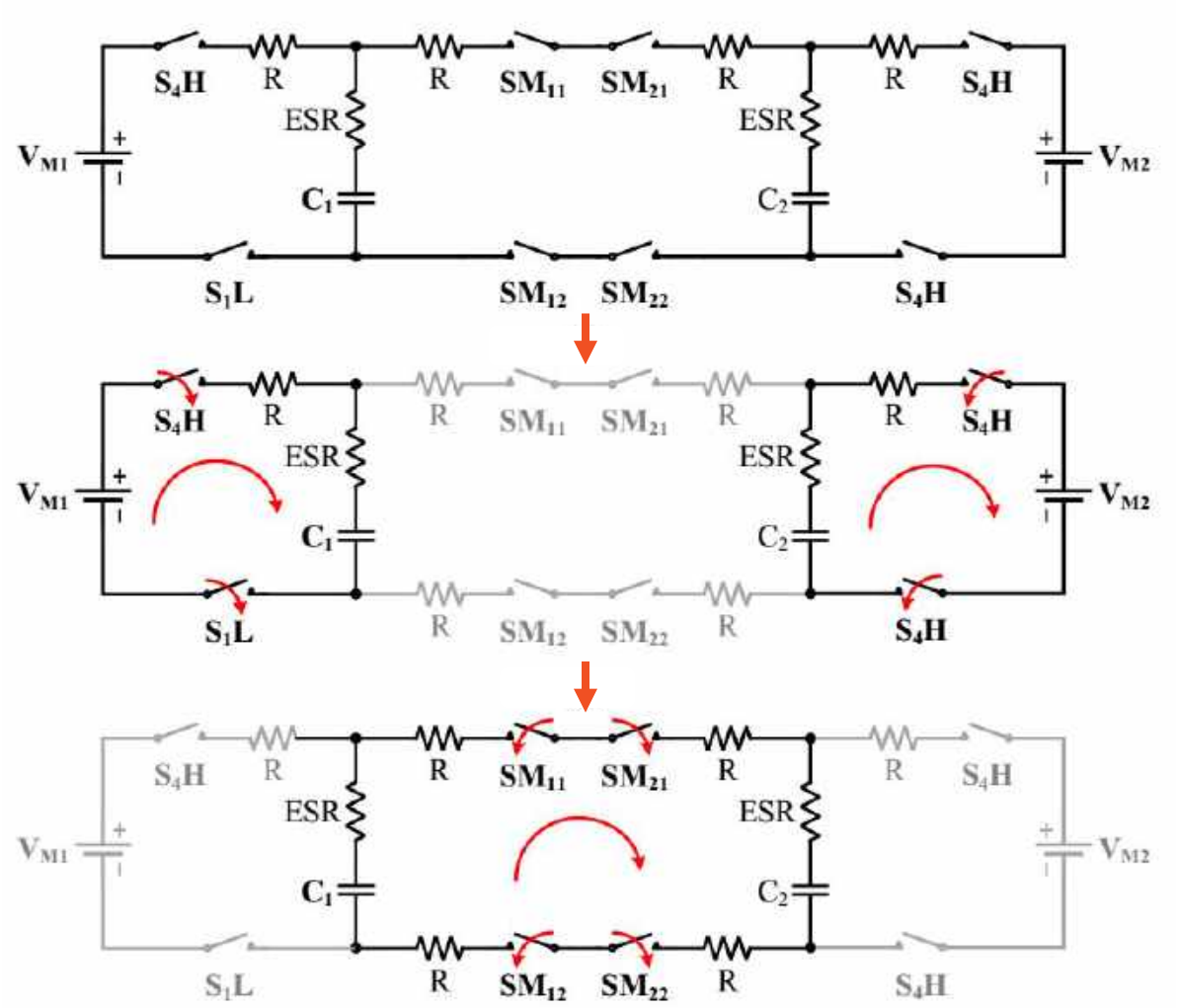
3. Conclusions and Future Works

4.1 Extended Version of SMC-E for Series-connected Modules



- Switch-matrix of SMC-E is modified for the module equalization.
- By connecting the balancing capacitor of the SMC-E, energy is transferred between modules.

4.1 Extended Version of SMC-E for Series-connected Modules



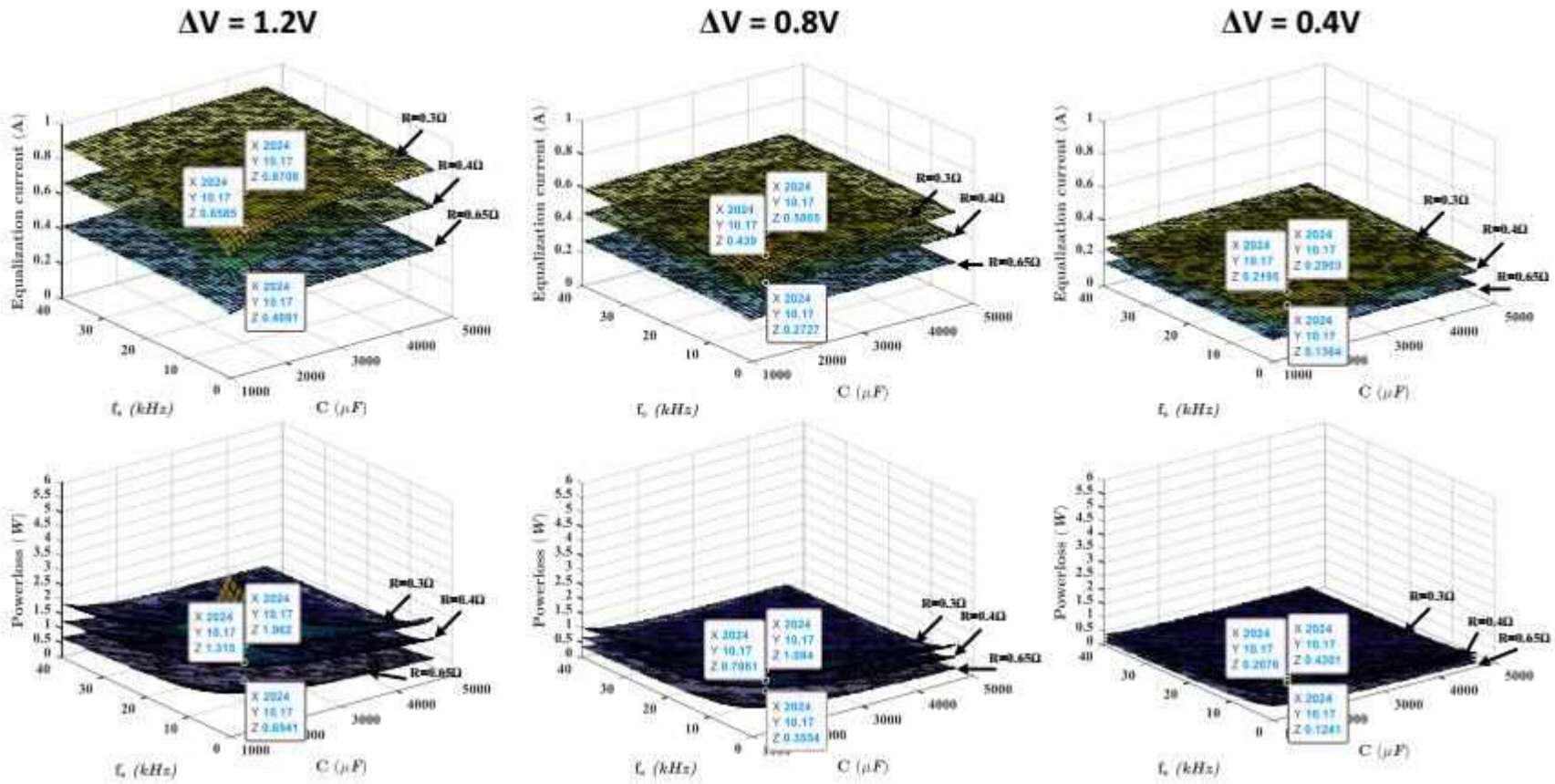
- Operating principle of the module equalization is almost similar to that of the cell-level.
- Average balancing current of the modules are calculated by:

$$V_{M\_avg} = \sum_{i=1}^{N} \frac{1}{N} V_{Mk},$$

$$I_{M1\_avg} = C f_s (V_{M1} - V_{M\_avg}) \left(1 - exp(\frac{-D}{f_s R_{loop} C_1})\right),$$

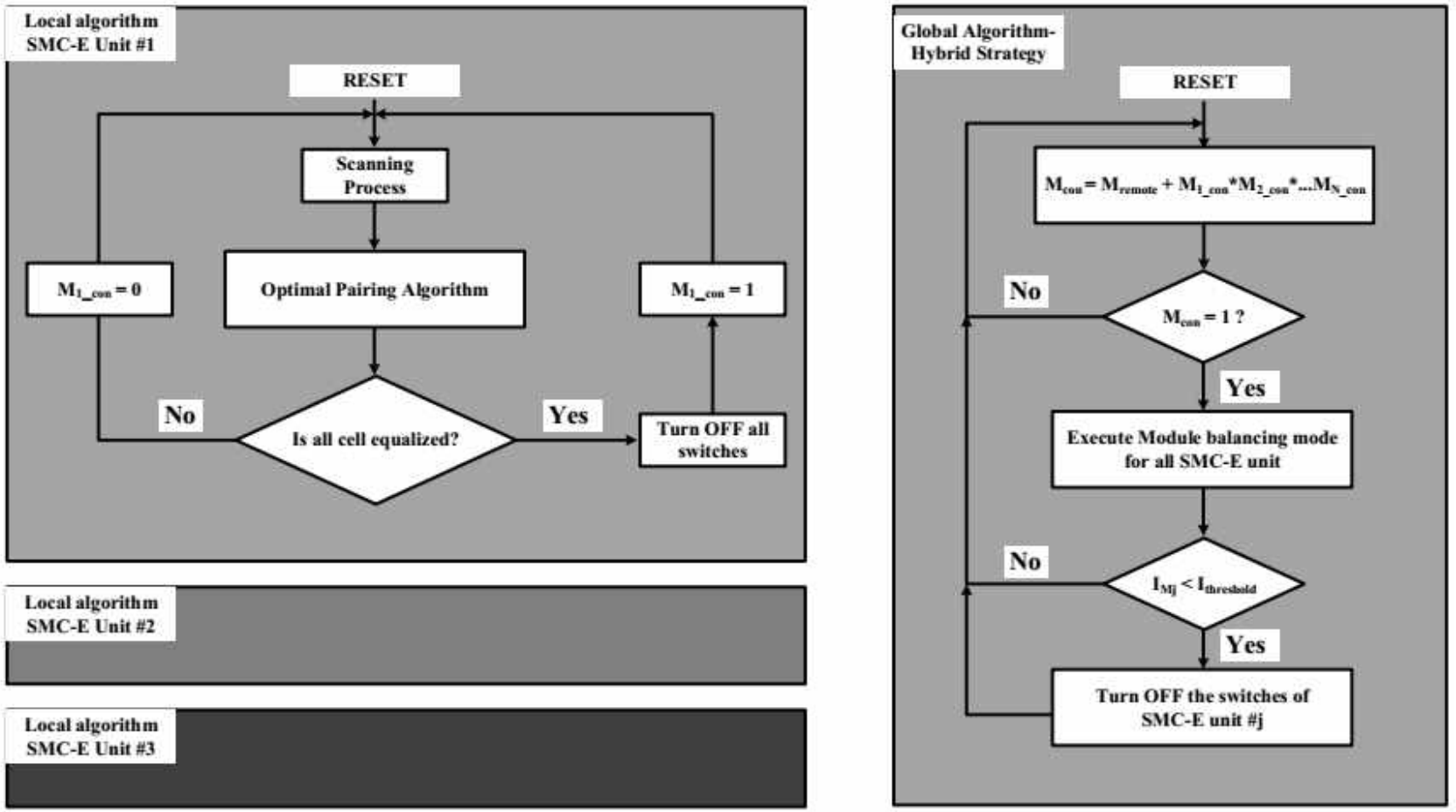
$$I_{M2\_avg} = C f_s (V_{M\_avg} - V_{M1}) \left(1 - exp(\frac{-D}{f_s R_{loop} C_2})\right) exp\left(\frac{-1}{2 f_s R_{loop} C_2}\right)$$

4.1 Extended Version of SMC-E for Series-connected Modules

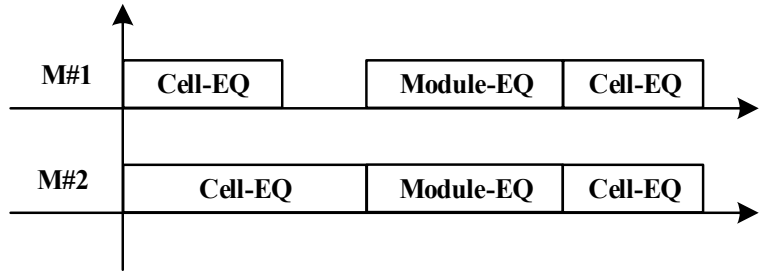


- Amplitude of average balancing current also depends on the voltage deviation and the resistance of the circuit.

4.1 Extended Version of SMC-E for Series-connected Modules

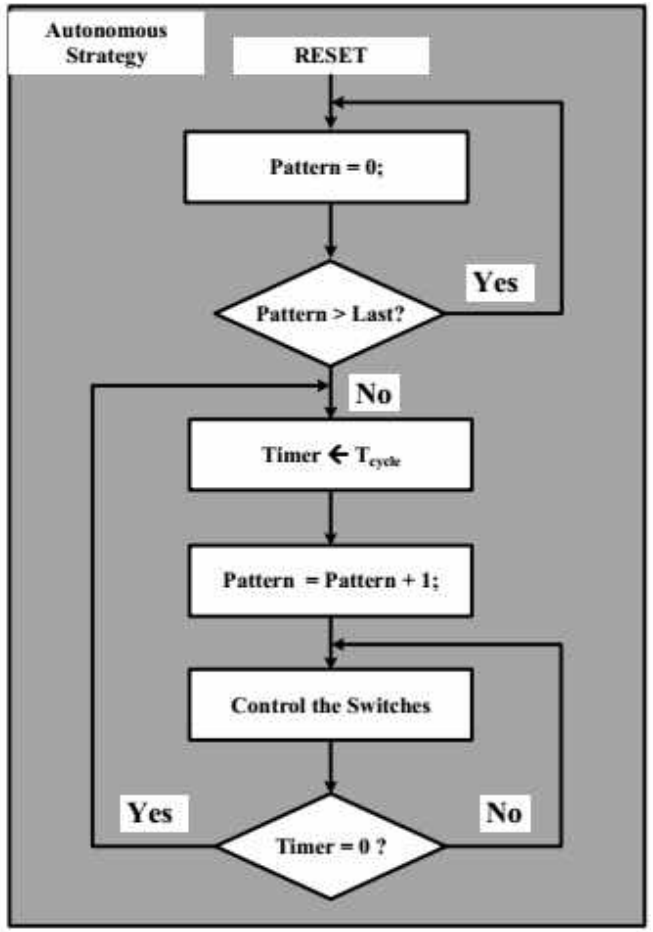


Hybrid Strategy

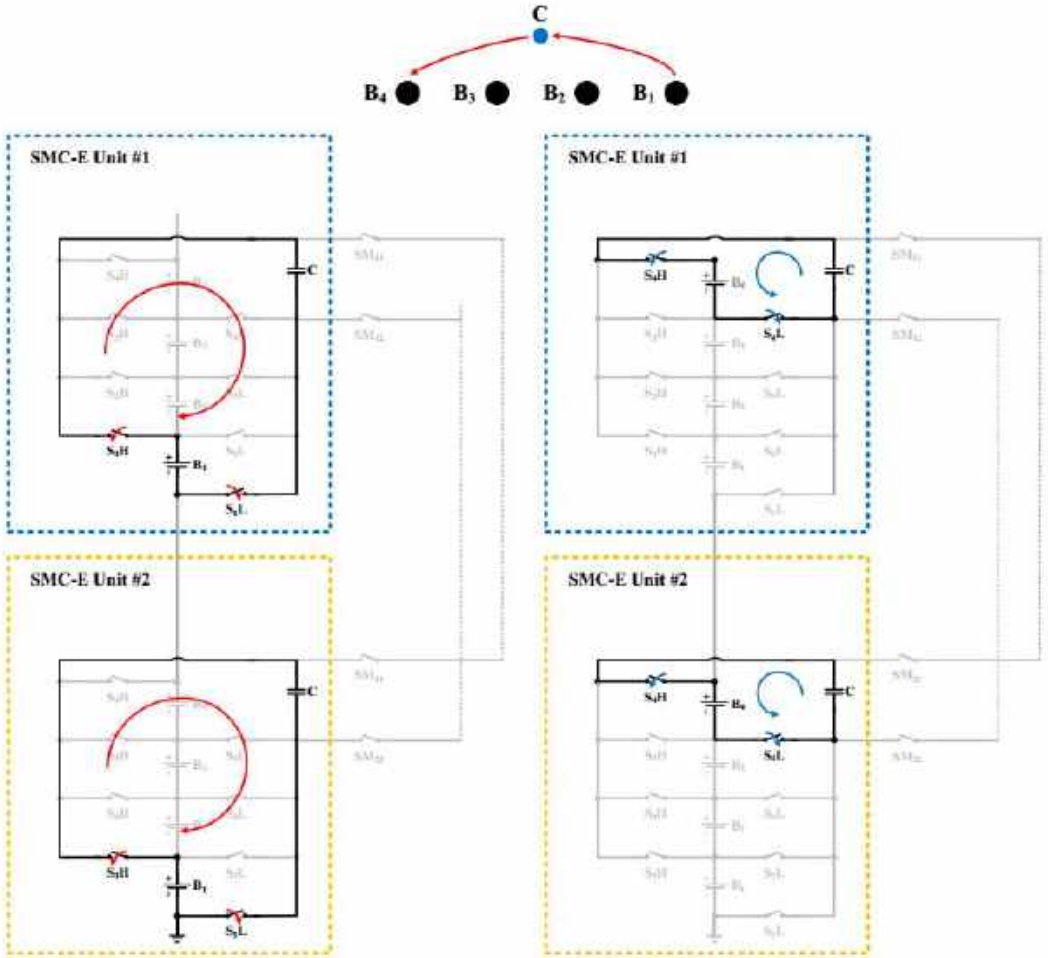


- **Optimal pairing algorithm** is utilized to inherit the advantage of the SMC-E **in cell level**.
- After **all cells inside each module is equalized**, module equalization is triggered.

4.1 Extended Version of SMC-E for Series-connected Modules

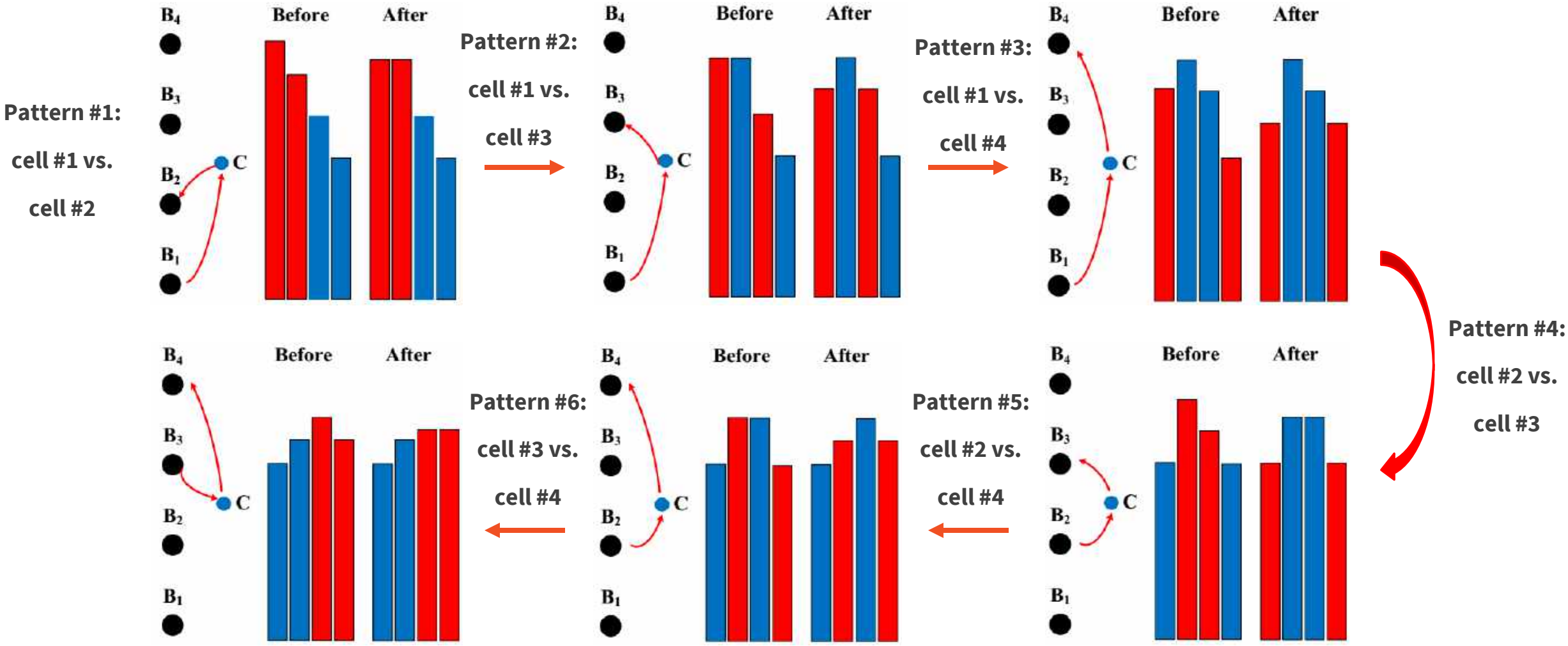


Autonomous Strategy

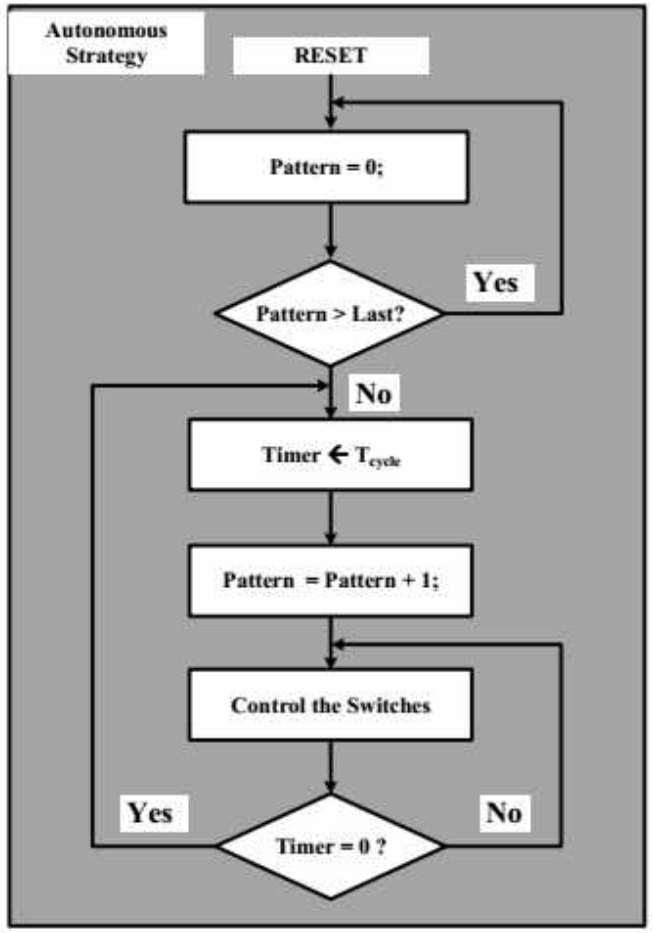


- **Cell-to-cell** equalization pattern.
- All combination is executed.

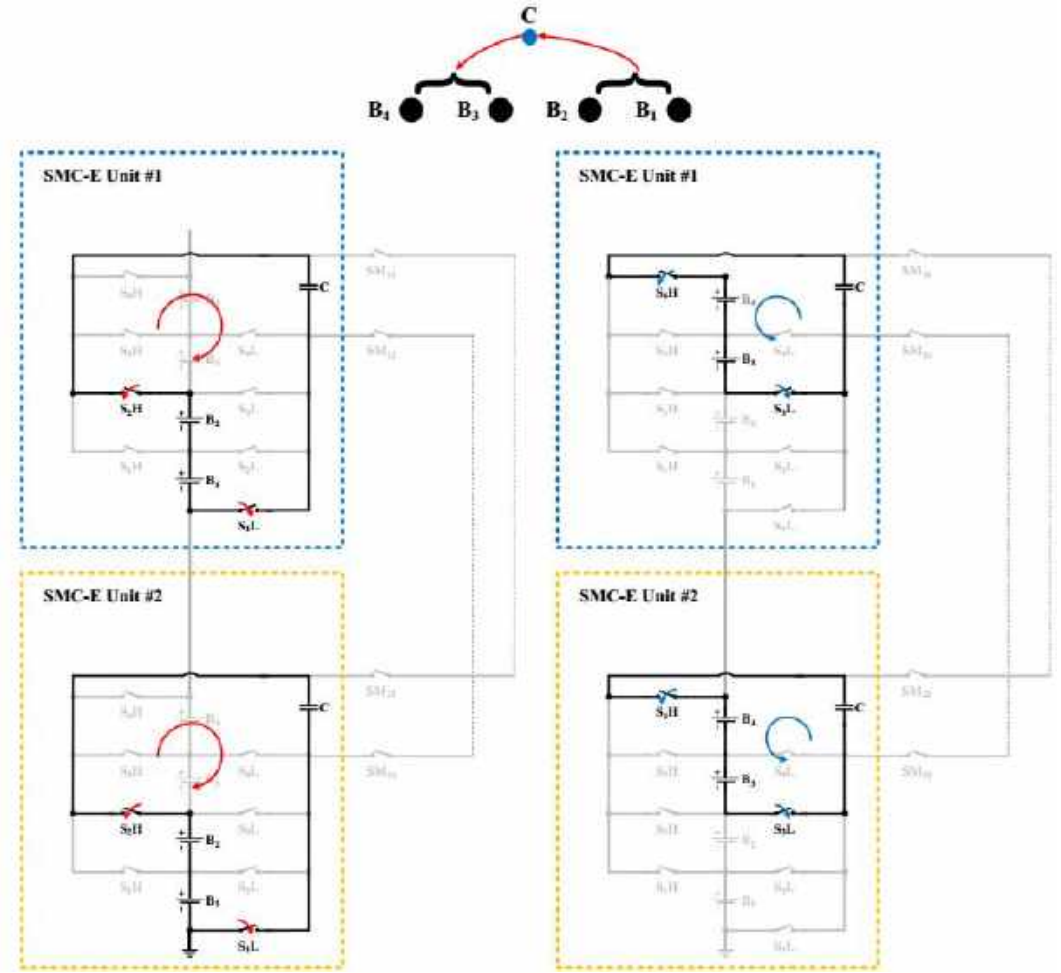
4.1 Extended Version of SMC-E for Series-connected Modules

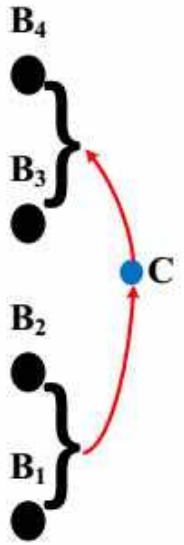


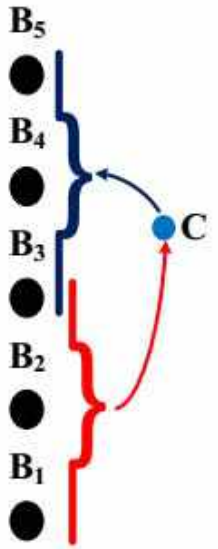
4.1 Extended Version of SMC-E for Series-connected Modules



Autonomous Strategy



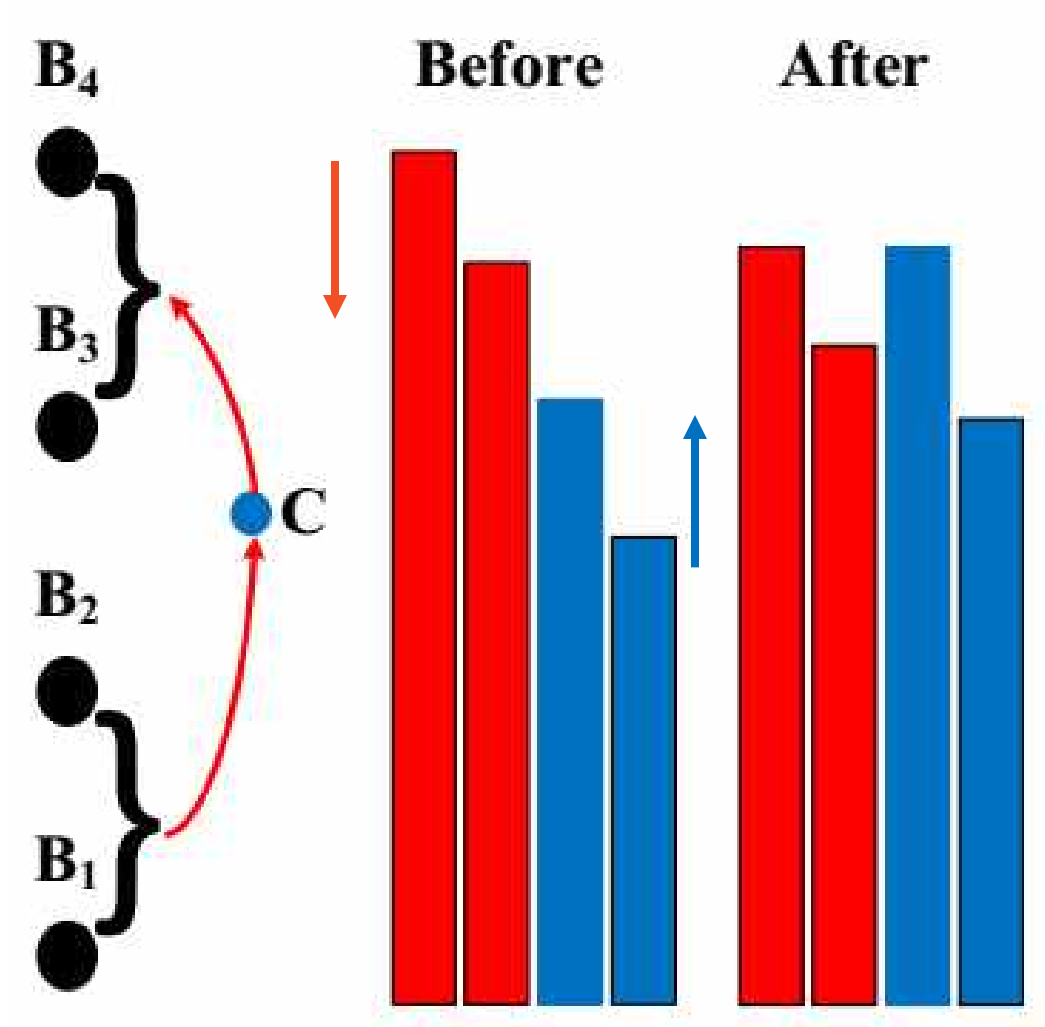




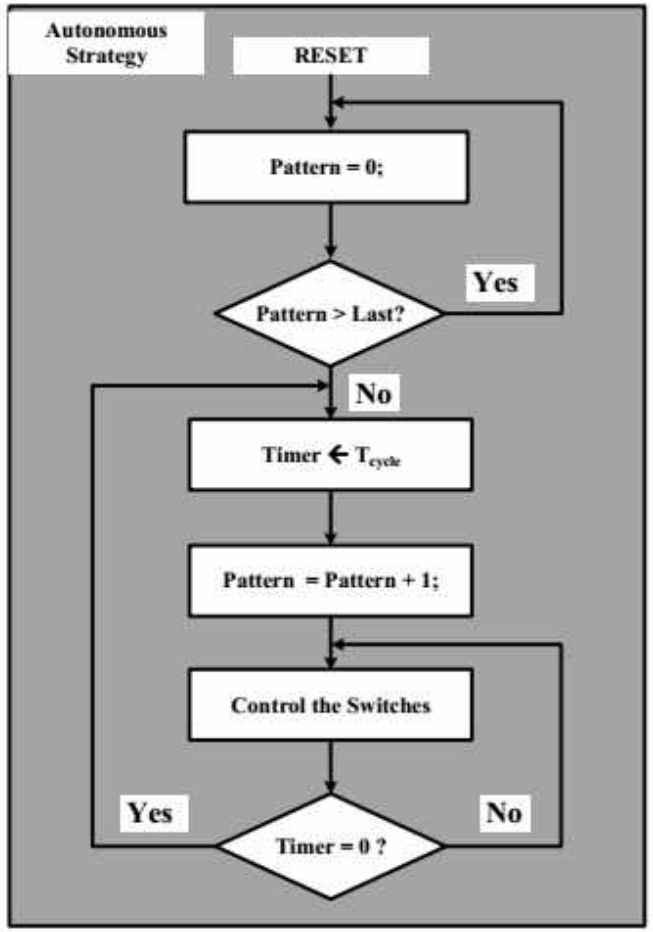
- **Sub-module to sub-module** equalization pattern.

4.1 Extended Version of SMC-E for Series-connected Modules

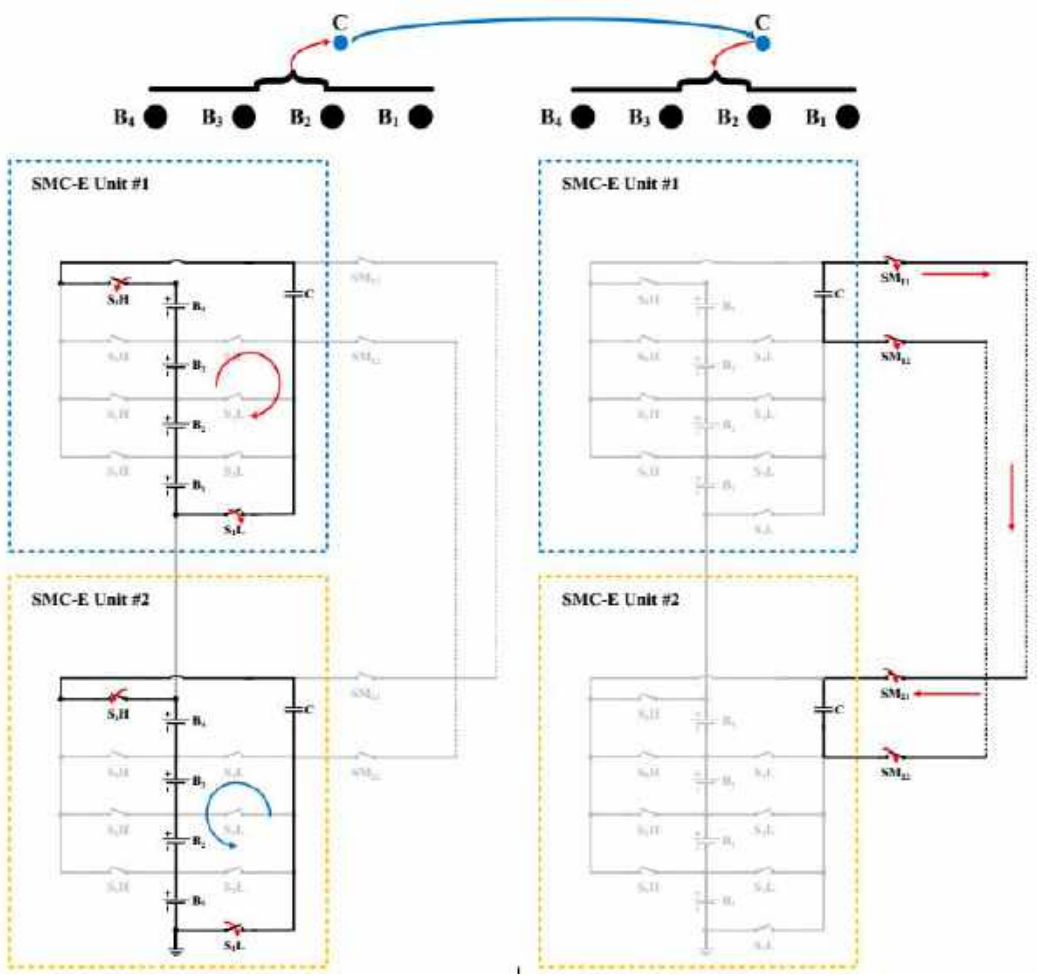
Pattern #7: Sub-module to Sub-module



4.1 Extended Version of SMC-E for Series-connected Modules



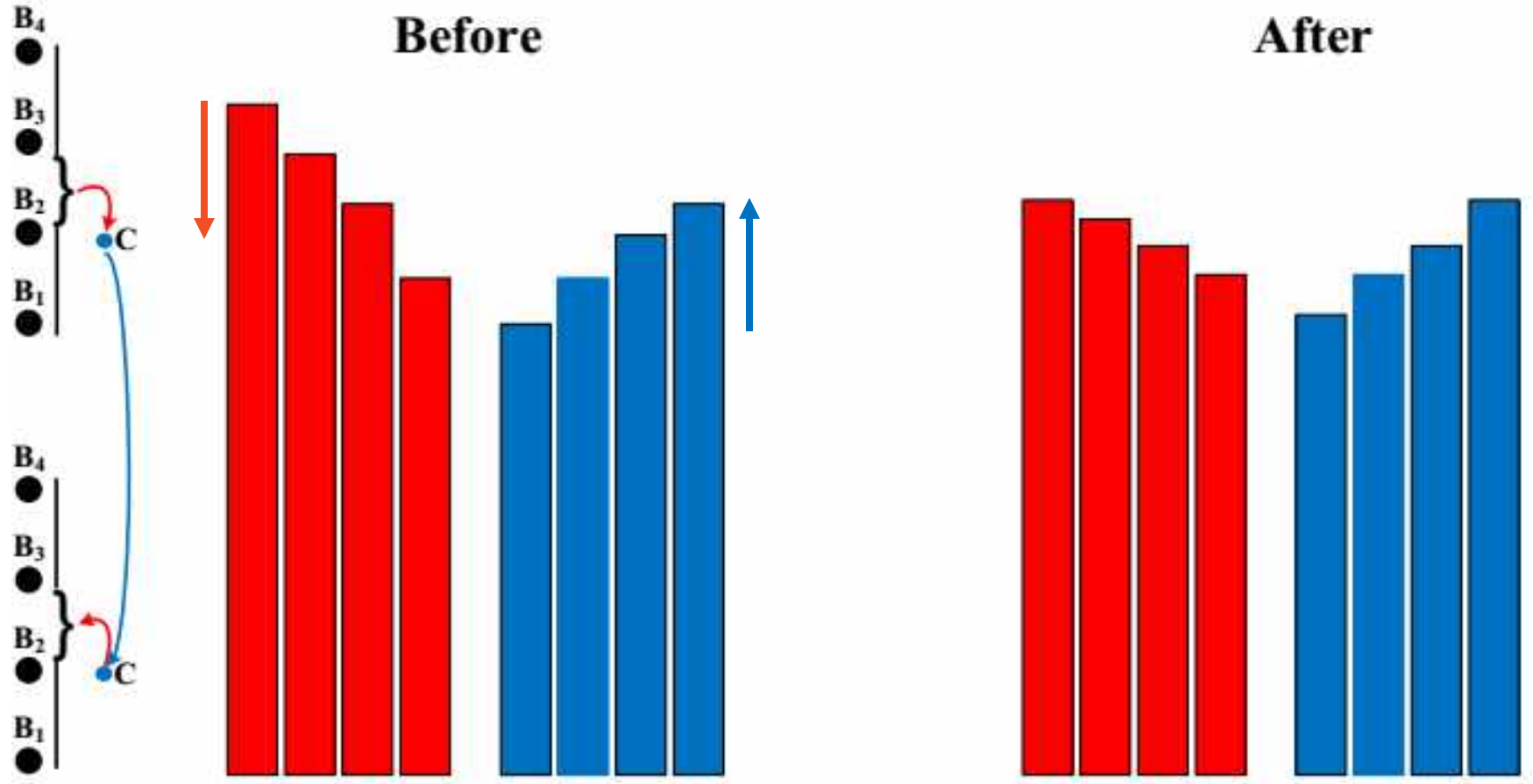
Autonomous Strategy



- **Module to Module** equalization pattern.

4.1 Extended Version of SMC-E for Series-connected Modules

Pattern #8: Module to Module



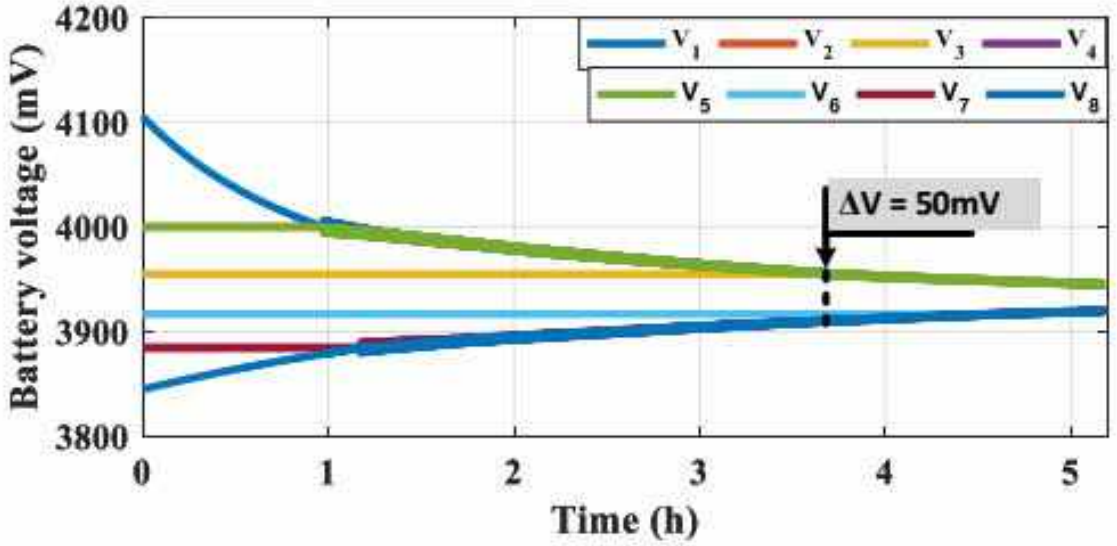
4.1 Extended Version of SMC-E for Series-connected Modules

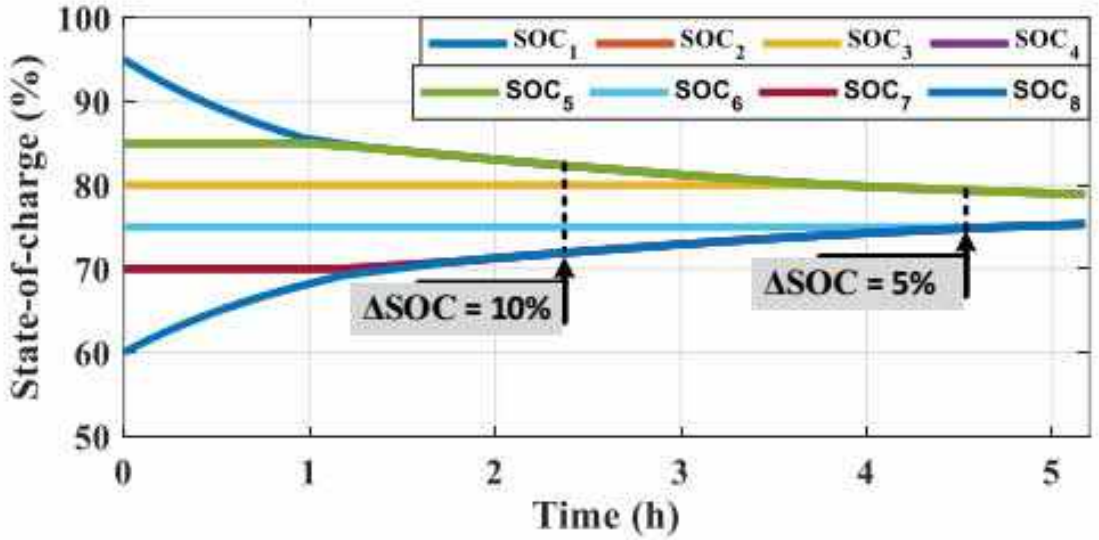
Table 4.2 TEST SETUP ON RTSS FOR SERIES MODULAR EQUALIZATION

Parameters	Setup
C_1 & C_2	$2048\mu F$
f_s	$10kHz$
R_{loop}	0.15Ω
Cell specs.	$3.6V - 2.6Ah$
Initial SOC level	$M_1: SOC_{1,2,3,4} = 95,\ 85,\ 80, 70\%$ | $M_2: SOC_{5,6,7,8} = 85,\ 75,\ 70, 60\%$

- **Real time simulation** is used to assess the performance of module equalization strategy.
- **Two modules** are tested, each module consists of **4 series connected cells**.
- **Two proposed equalization strategies** are compared with the **optimal pairing algorithm** for 8S1P string.

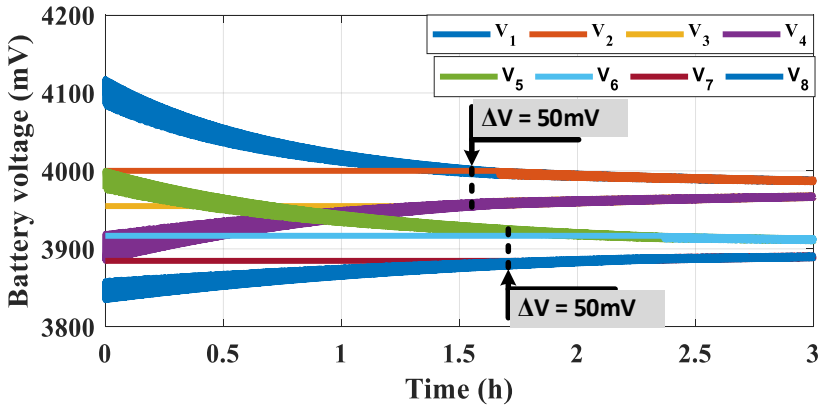
4.1 Extended Version of SMC-E for Series-connected Modules

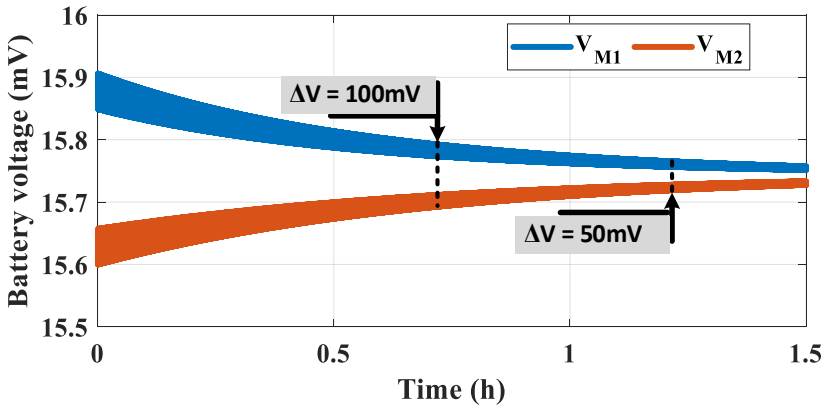


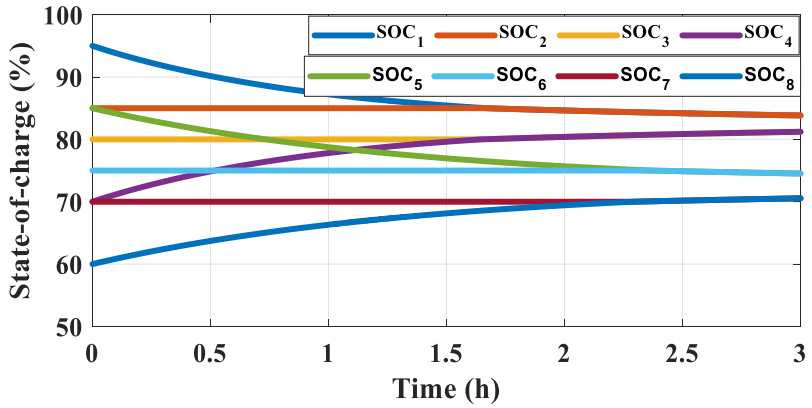


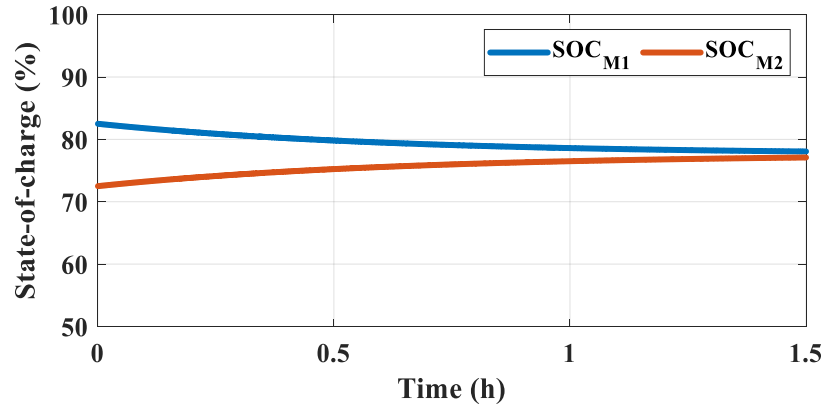
- **Optimal pairing algorithm** for **8S1P string** requires **5.2h** to balance the cells within 30mV of voltage deviation and 4% of SOC difference.
- Calculated **DoSE, DoVE, SR_V, and SR_{SOC} are 84%, 85.6%, 42.3mV/h, and 4.04%/h**, respectively.

4.1 Extended Version of SMC-E for Series-connected Modules



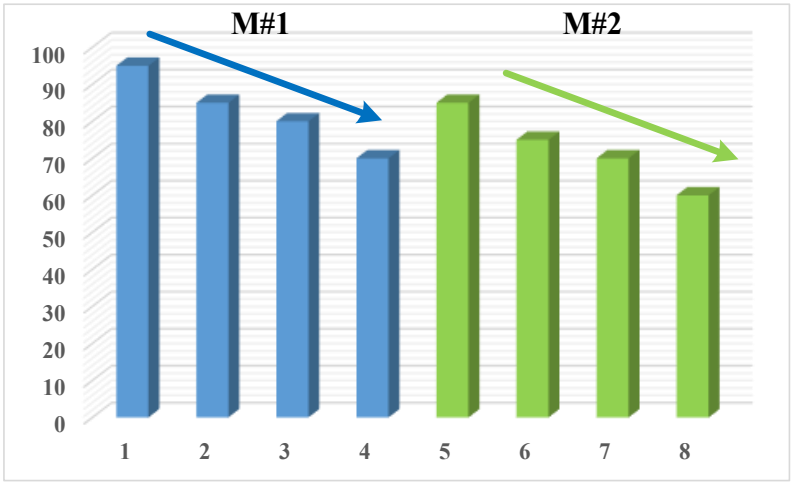




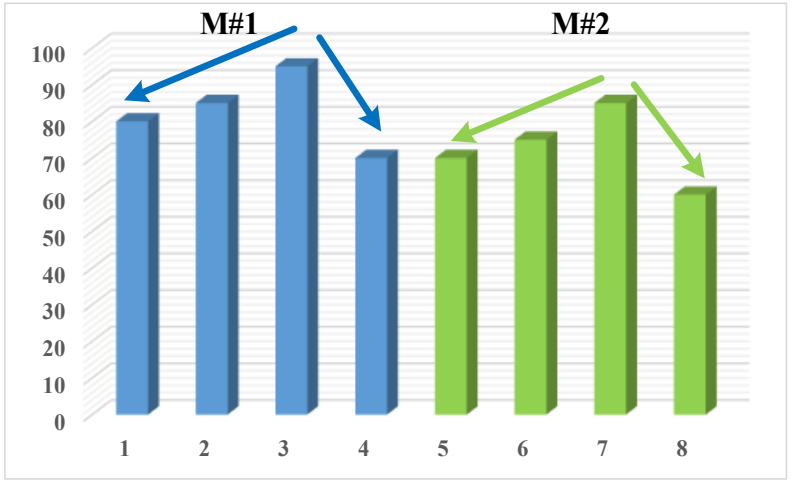


- **Cell equalization and Module equalization** processes are **separately executed**.
- After 4.5h, all cells are equalized within **25mV voltage deviation**, and **1% of SOC difference**.
- Calculated **SR_V, and SR_{SOC} are 50mV/h, and 4.9%/h**, respectively.

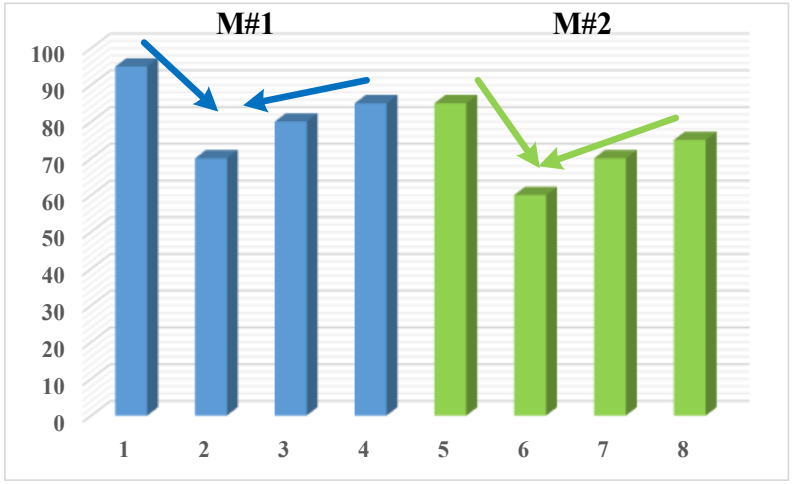
4.1 Extended Version of SMC-E for Series-connected Modules



Descending Order



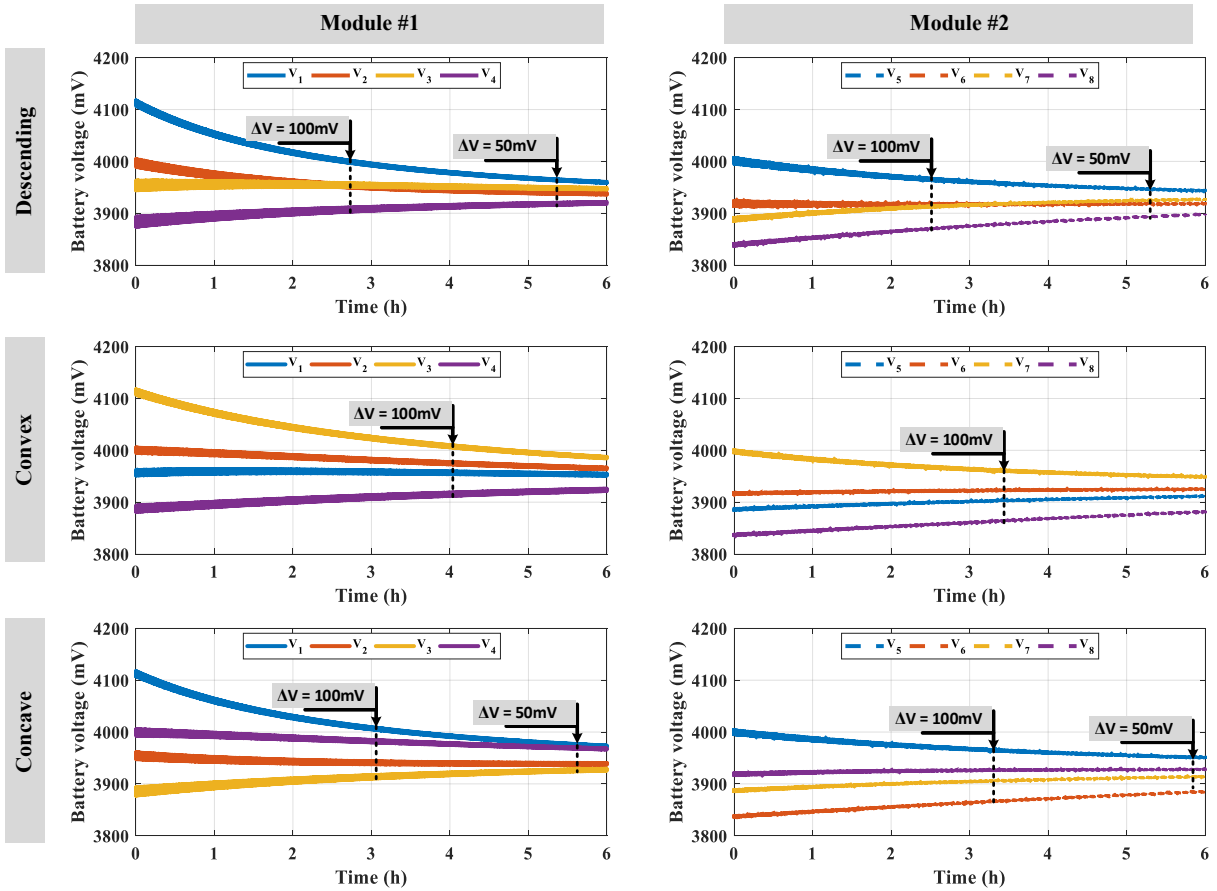
Convex Order



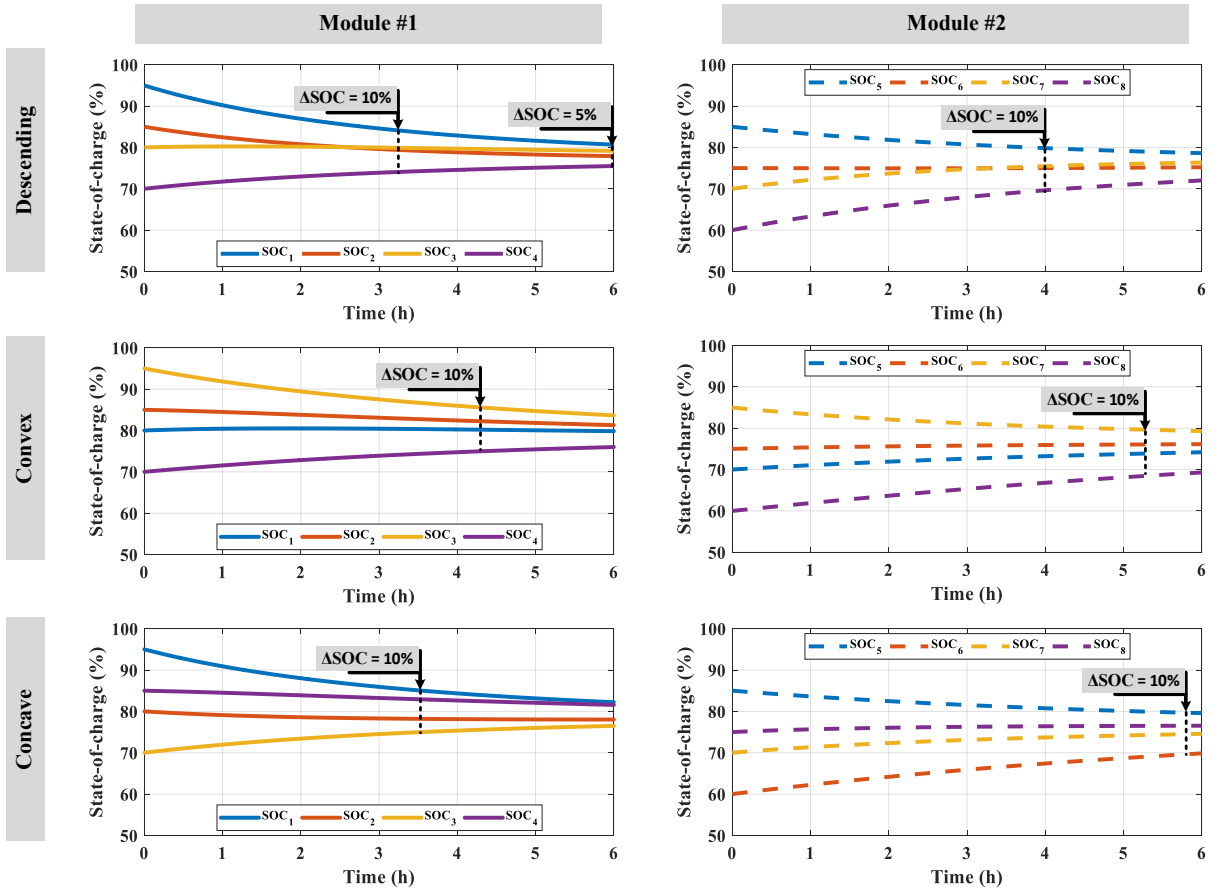
Concave Order

- **Autonomous strategy** is tested under **three different test scenarios** to **assess the performance and stability.**
- **The equalization capability and equalization speed are assessed.**

4.1 Extended Version of SMC-E for Series-connected Modules

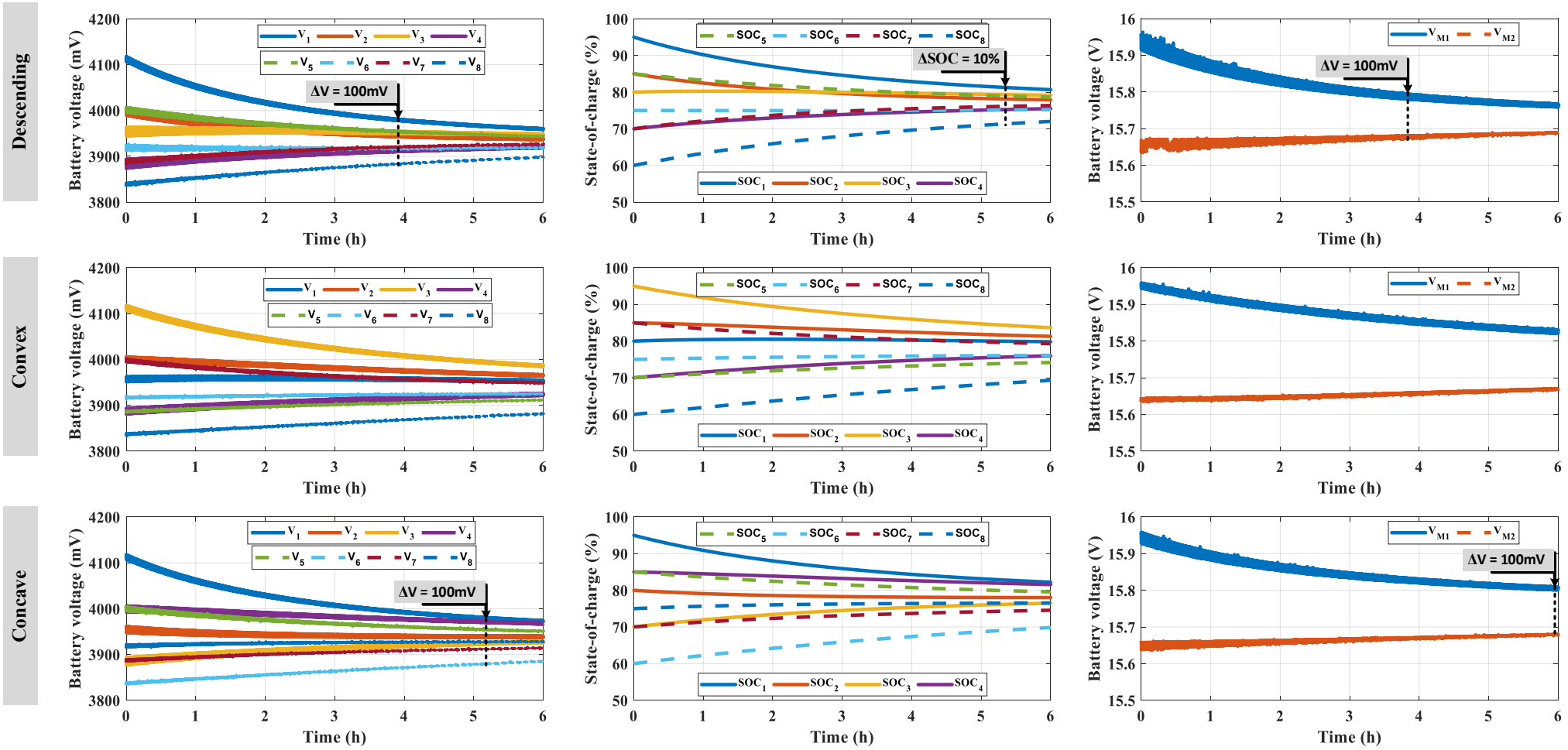


Voltage Profile



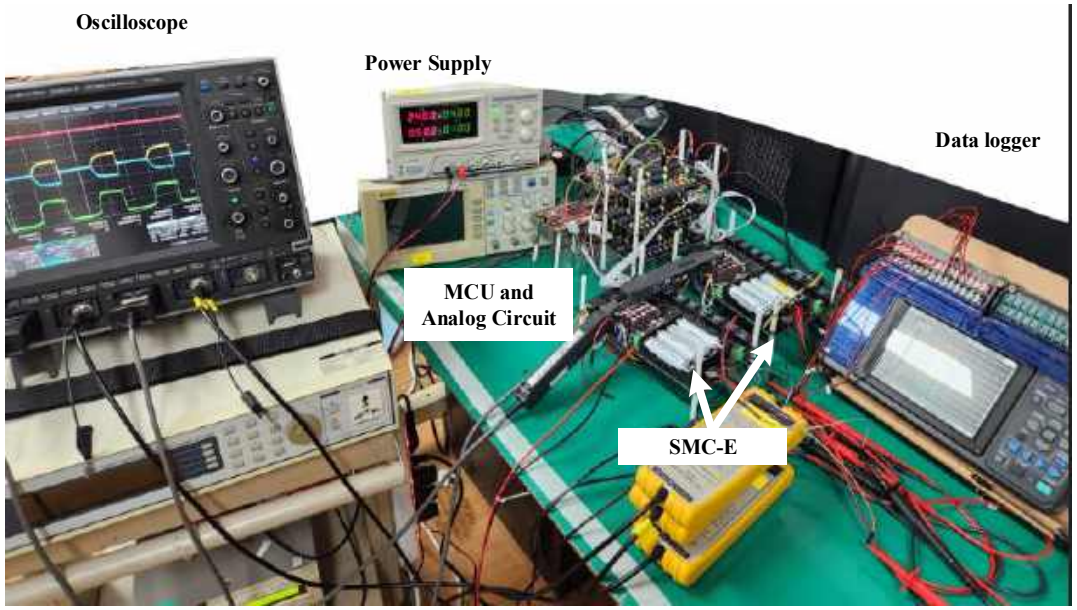
SOC Profile

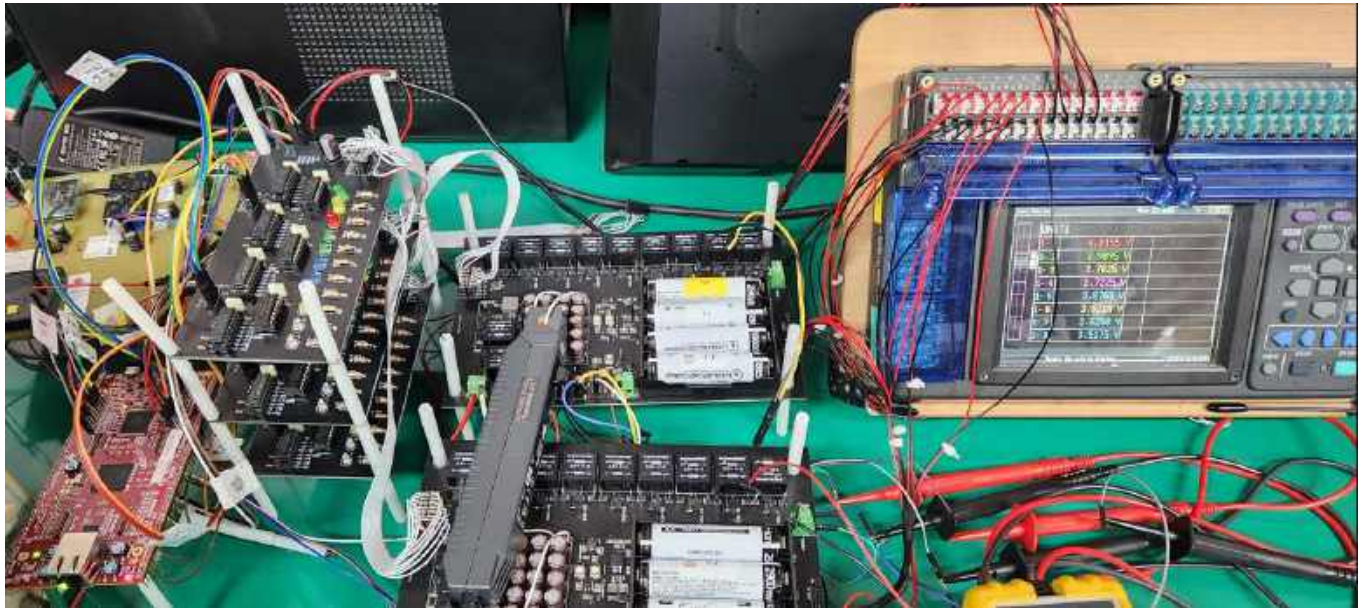
4.1 Extended Version of SMC-E for Series-connected Modules



Voltage Profile of the Cells | SOC Profile | Voltage Profile of modules

4.1 Extended Version of SMC-E for Series-connected Modules

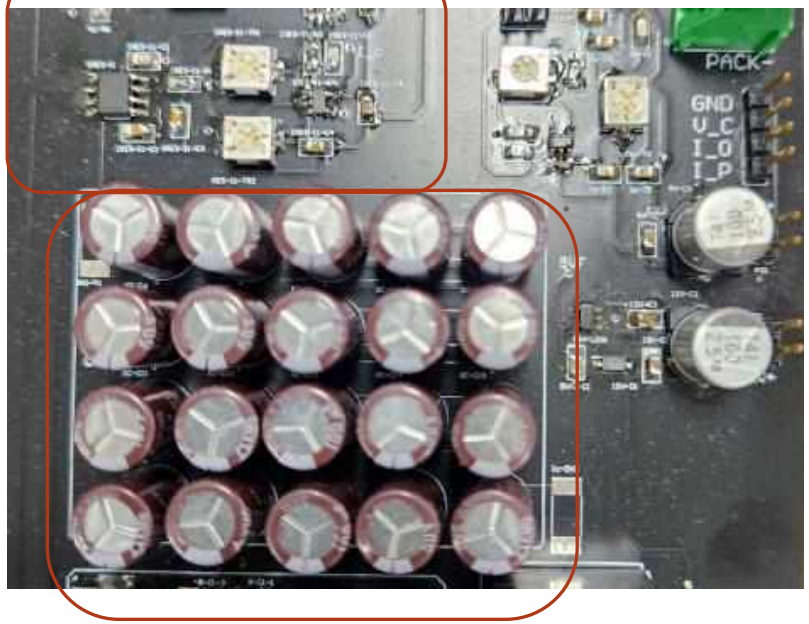




- **A prototype of SMC-E** for **4S1P battery string is made.**
- **Two SMC-E** are used to assess **the cell and module equalization.**
- **Waveform signal** is captured by the **oscilloscope** while the **voltage profile** is recorded by **a data logger.**

4.1 Extended Version of SMC-E for Series-connected Modules

Current Sensor



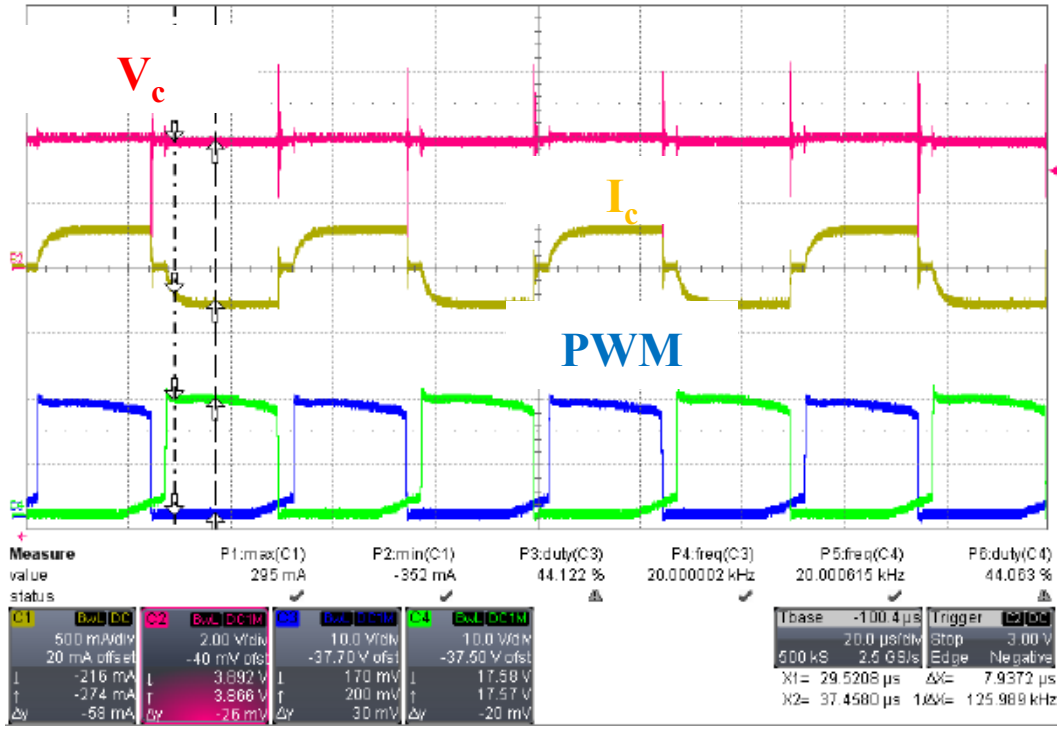
20x100uF Capacitor

Switch-matrix and Gate Driver

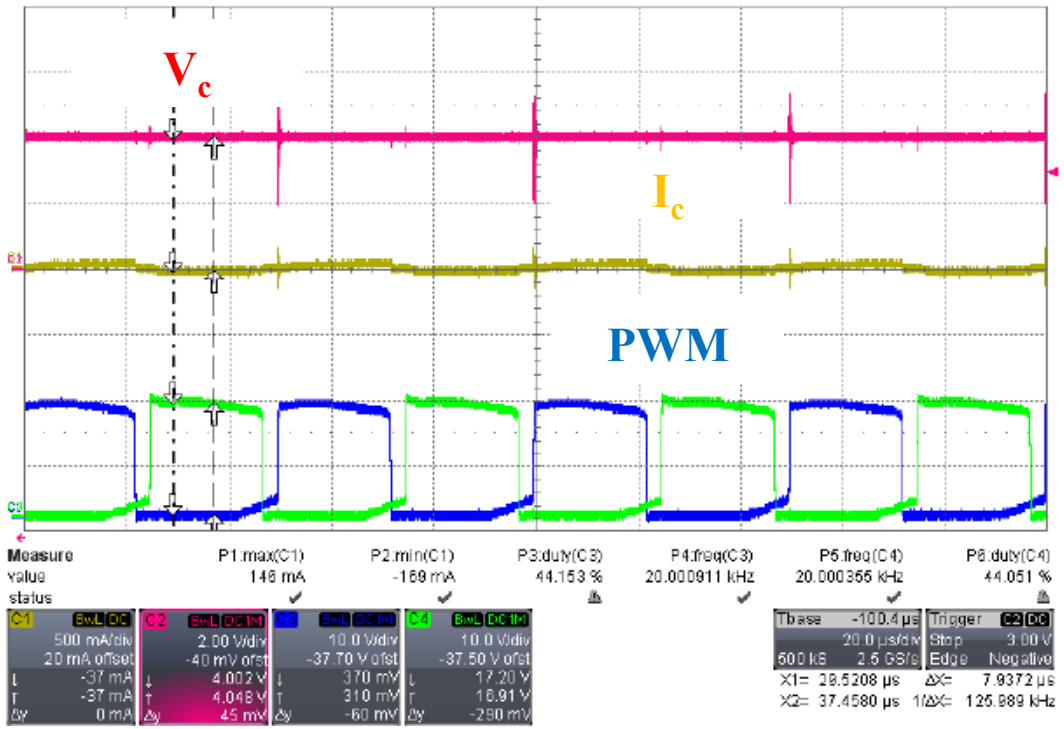
Parameter	Value
C	2205 uF
$R_{circuit}$	≈ 0.565 Ω
MOSFET	NVMFD5485NL dual N-channel 60V-20A-40mΩ
Pulse Trans.	Schurter ILR-11-0001
Gate driver	Microchip TC-4420
Cell	Samsung SDI ICR18650-30A (Megacanon 2.9Ah)

Balancing Capacitance and internal resistance

4.1 Extended Version of SMC-E for Series-connected Modules

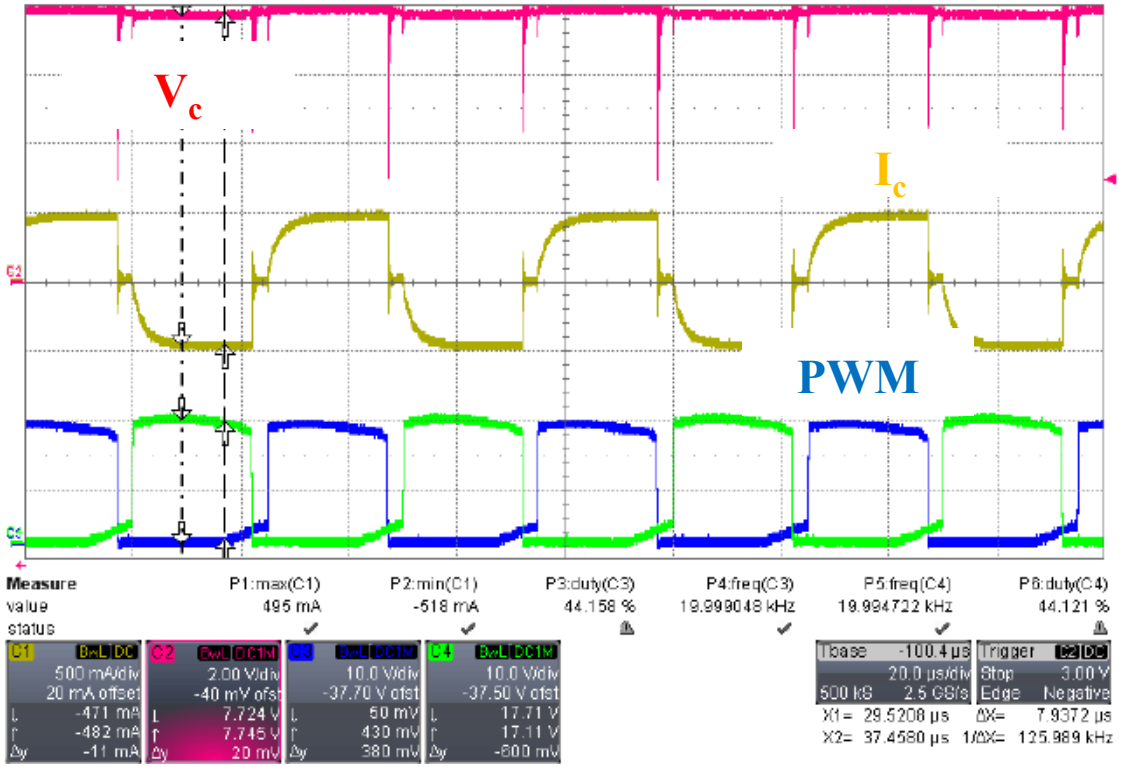


$\Delta V = 250mV$

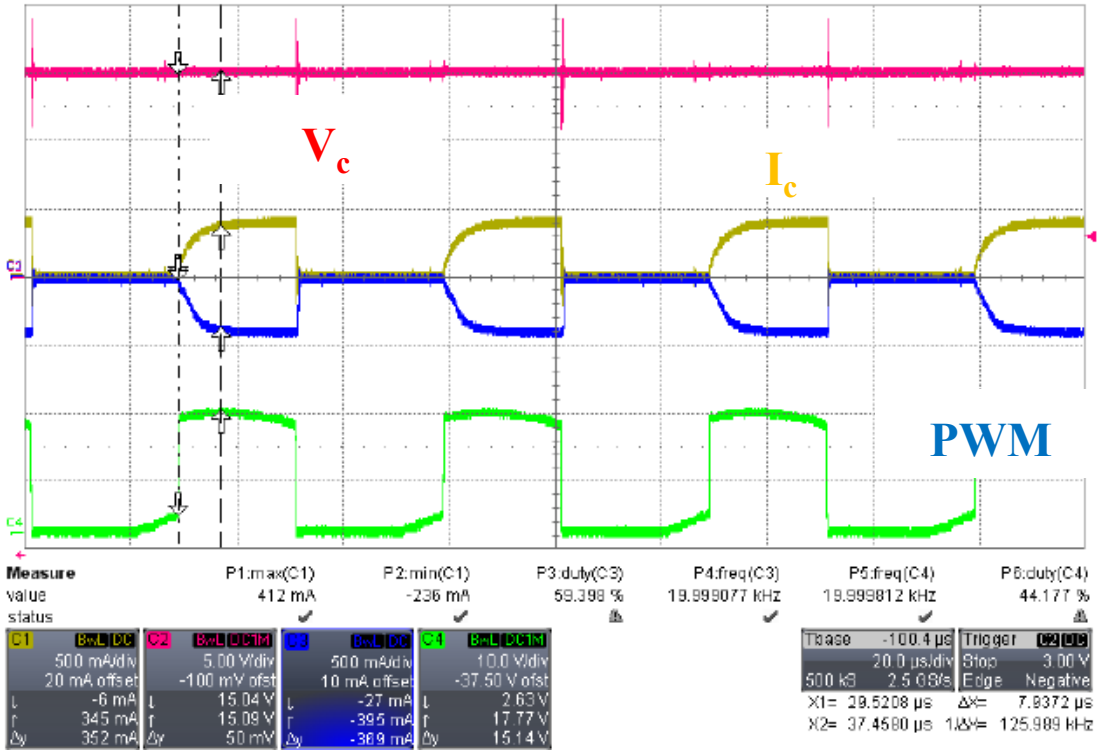


$\Delta V = 100mV$

4.1 Extended Version of SMC-E for Series-connected Modules

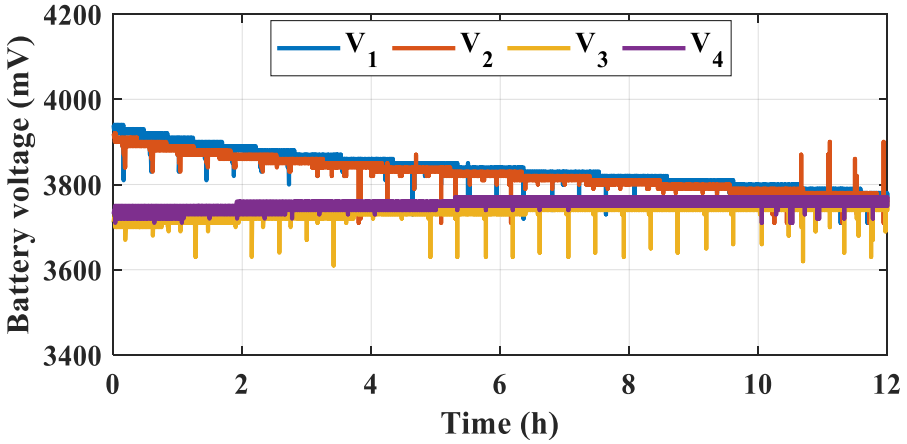


Sub-module to Sub-module

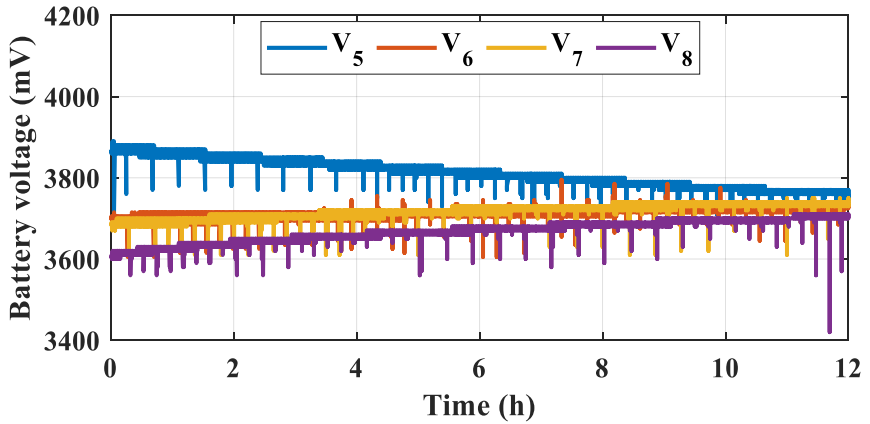


Module to Module

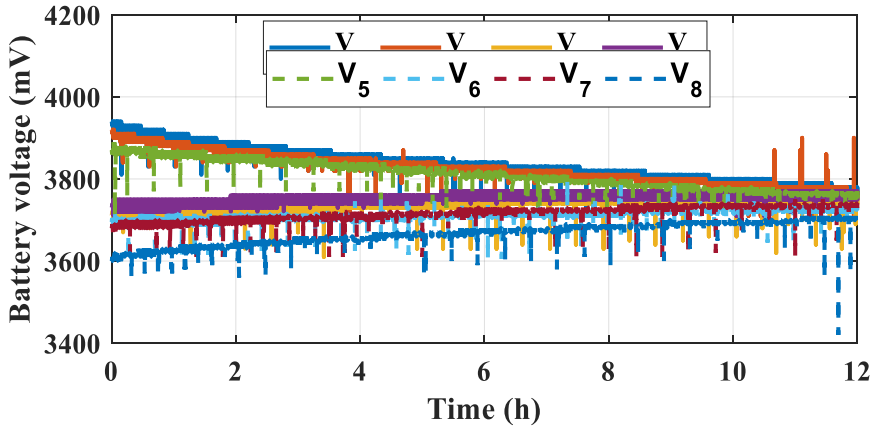
4.1 Extended Version of SMC-E for Series-connected Modules



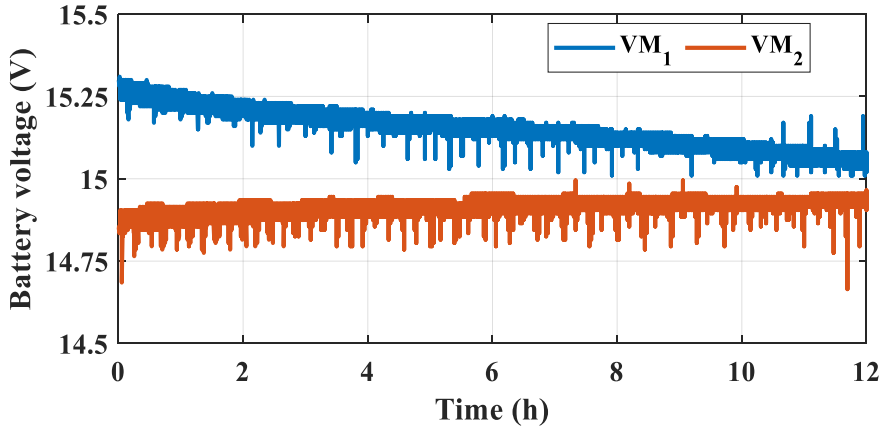
Voltage Profile of the Cells in Module 1



Voltage Profile of the Cells in Module 2

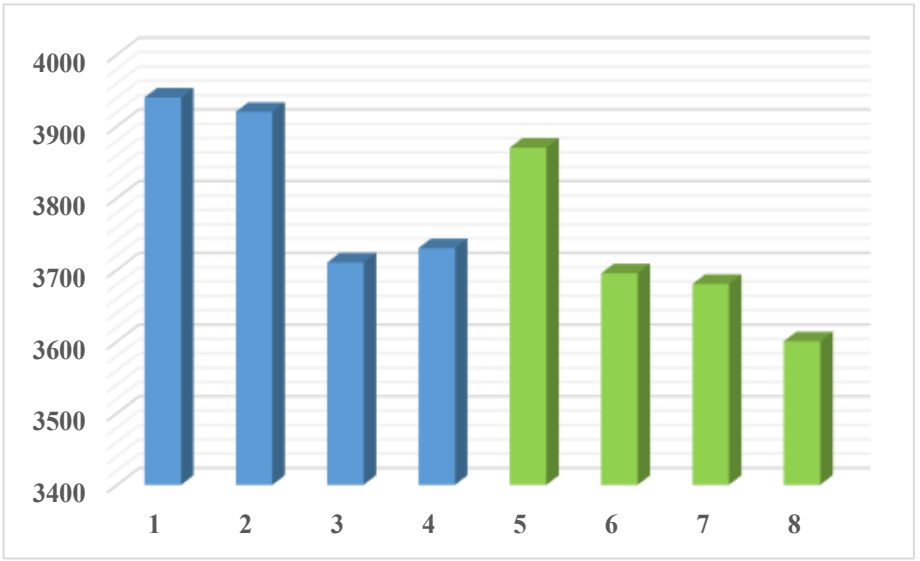


Voltage Profile all Cells

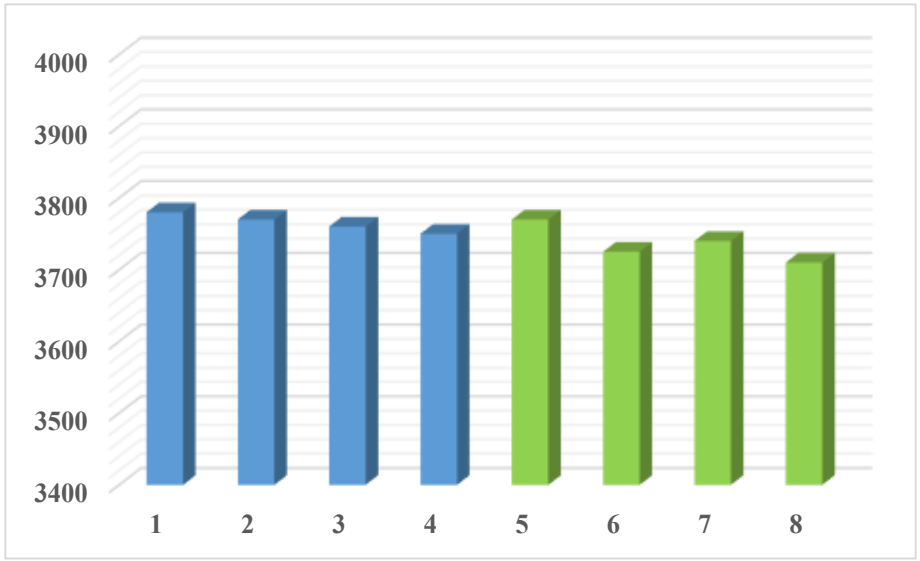


Voltage Profile Modules

4.1 Extended Version of SMC-E for Series-connected Modules



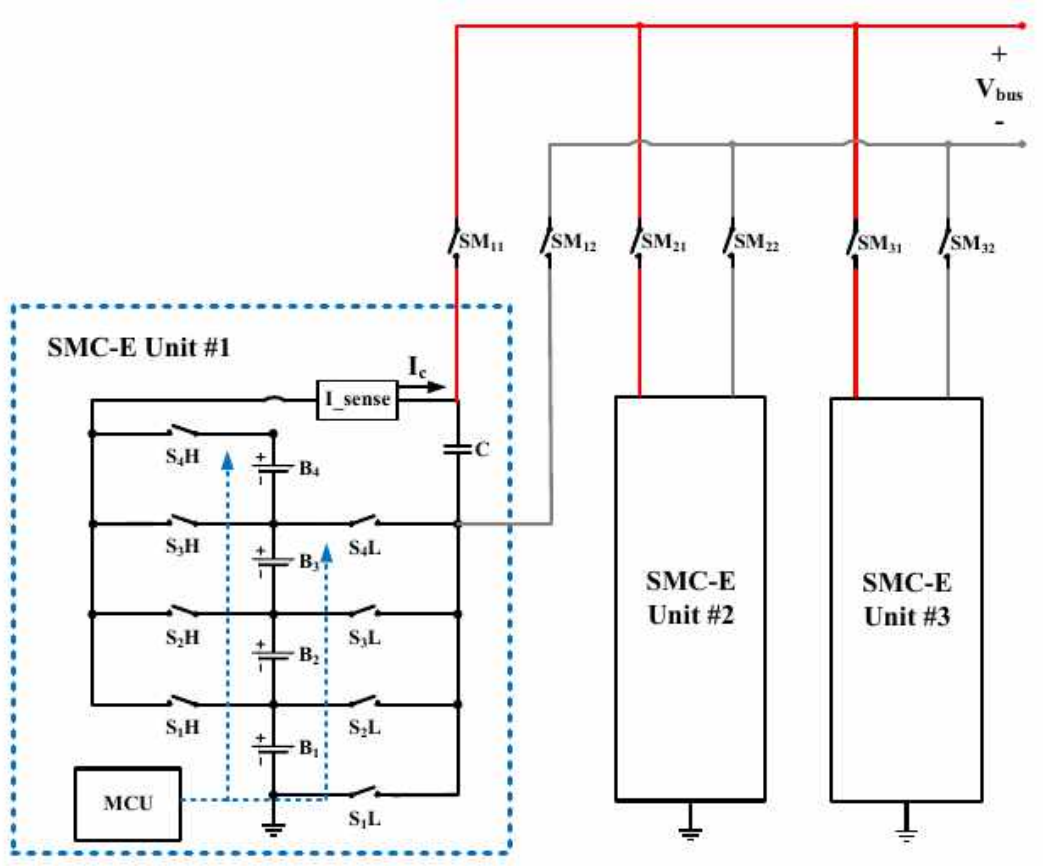
Before the Equalization



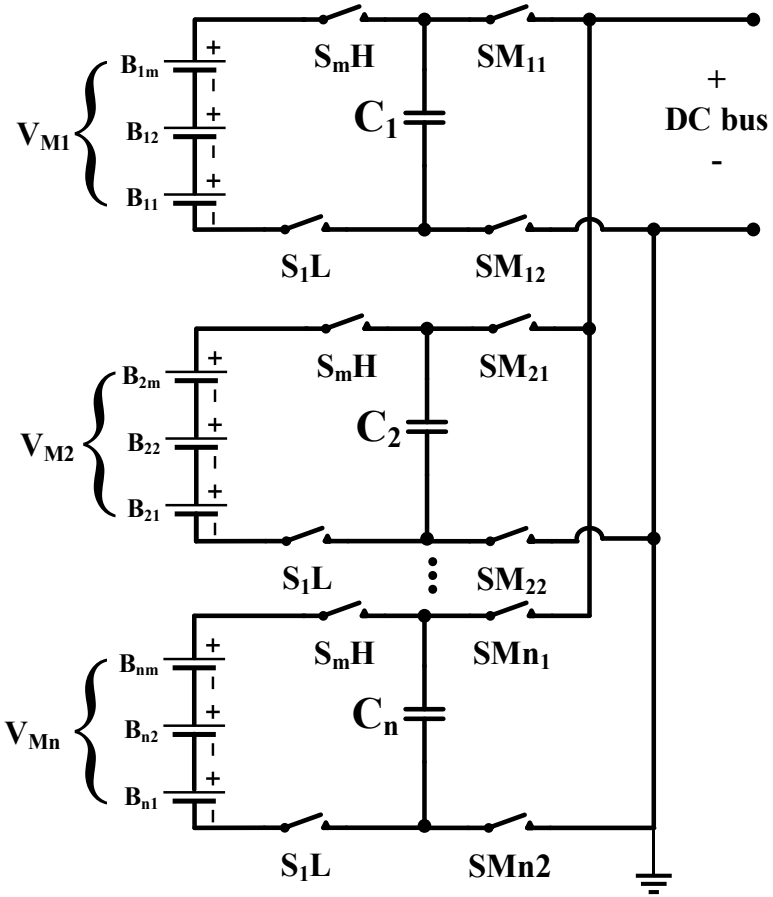
After the Equalization

	#1	#2	#3	#4	#5	#6	#7	#8	ΔV_all	ΔV_M_1	ΔV_M_2
Before (mV)	3940	3920	3710	3730	3870	3695	3680	3600	340	230	270
After (mV)	3780	3770	3760	3750	3770	3725	3740	3710	70	30	60

4.2 Extended Version of SMC-E for Parallel-connected Modules

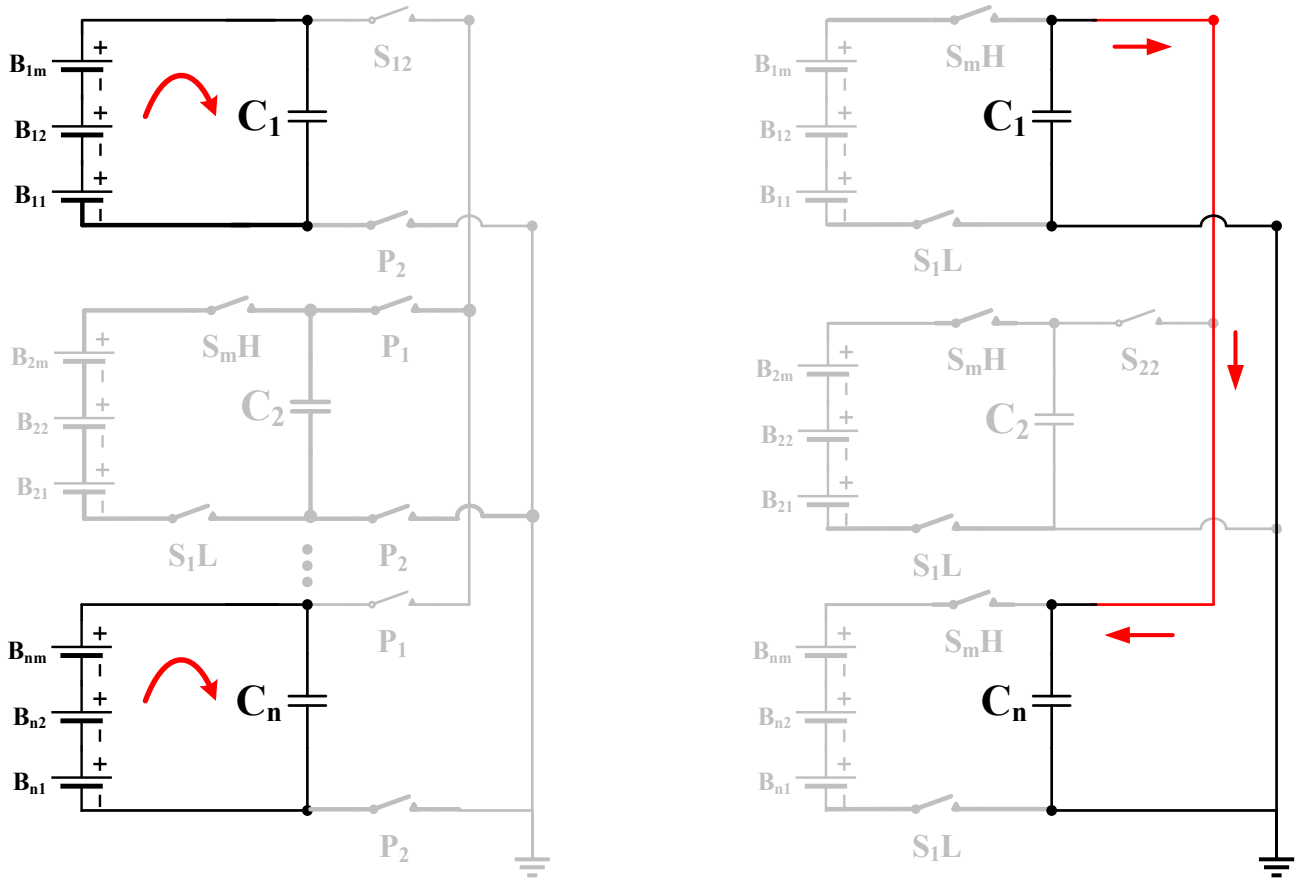


Concept



Equivalent Circuit

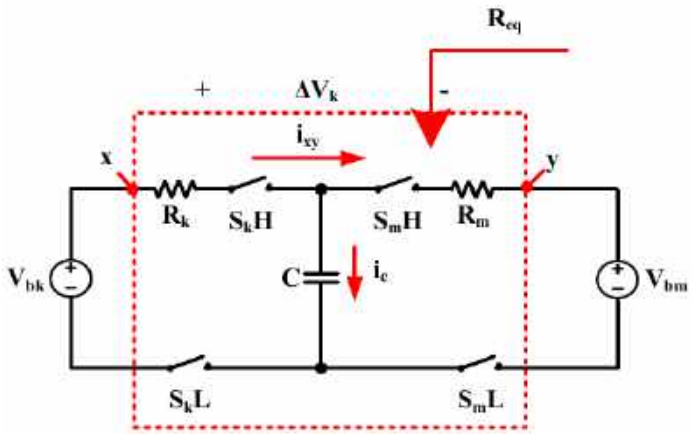
4.2 Extended Version of SMC-E for Parallel-connected Modules



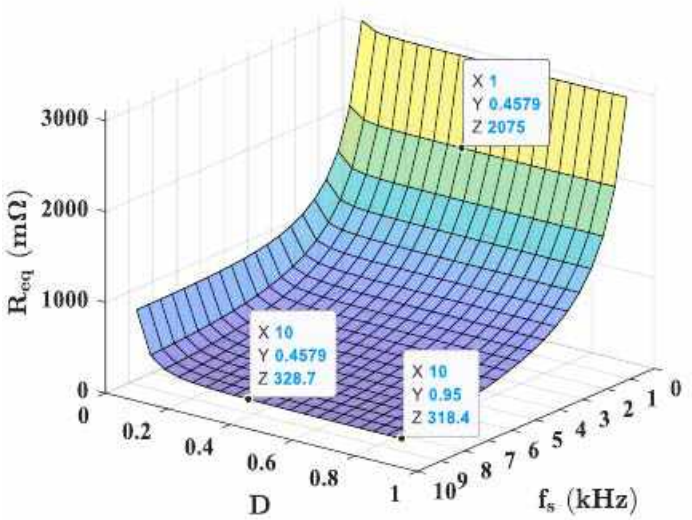
Equalization Strategy in IDLE mode

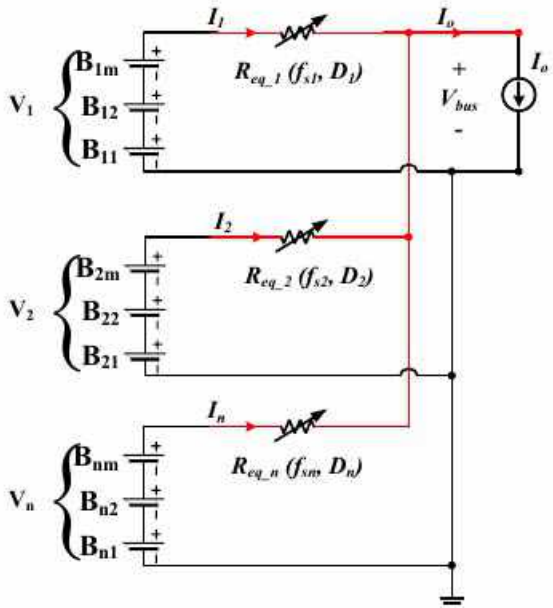
- **In IDLE mode,** equalization strategy is similar to in Series-connected modules.
- Module voltages are monitored to detect the highest voltage module and the lowest voltage module.
- Equalization process between two modules.

4.2 Extended Version of SMC-E for Parallel-connected Modules



$$R_{eq} = \frac{1}{f_s C} \frac{e^{\frac{D_1}{f_s \tau_k}} e^{\frac{D_2}{f_s \tau_m}} - 1}{\left(e^{\frac{D_1}{f_s \tau_k}} - 1\right)\left(e^{\frac{D_2}{f_s \tau_m}} - 1\right)}.$$





$$Z_1 I_1 - Z_2 I_2 = V_1 - V_2$$

$$Z_1 I_1 - Z_3 I_3 = V_1 - V_3$$

...

$$Z_1 I_1 - Z_n I_n = V_1 - V_n$$

$$I_1 + I_2 + I_3 + \ldots + I_n = I_0,$$

- By regulating the switching frequency, the branch impedance can be adjusted.
- The branch current can be managed to balance the energy level of the modules.

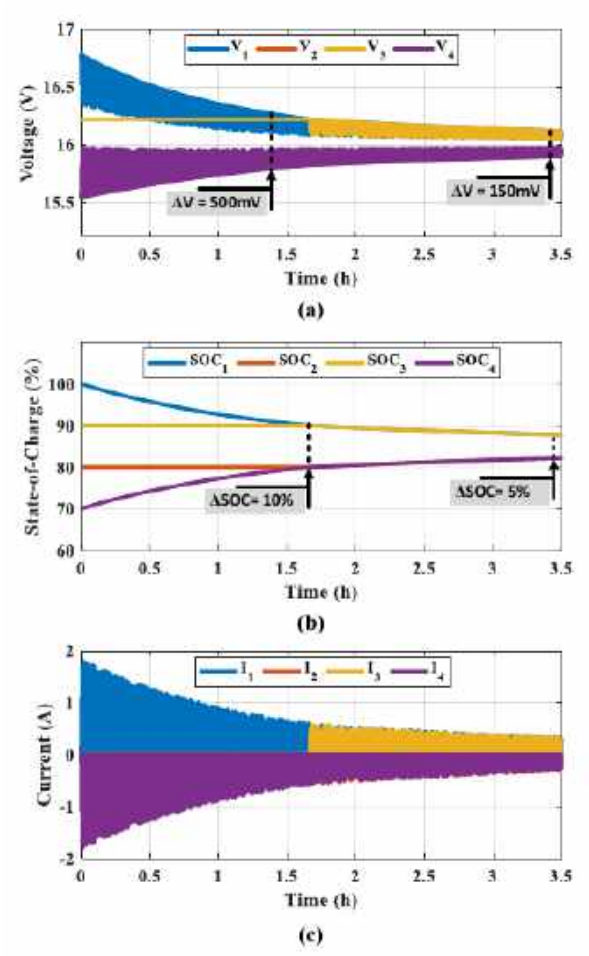
4.2 Extended Version of SMC-E for Parallel-connected Modules

Table 4.3 TEST SETUP ON RTSS FOR PARALLEL CONNECTED MODULES

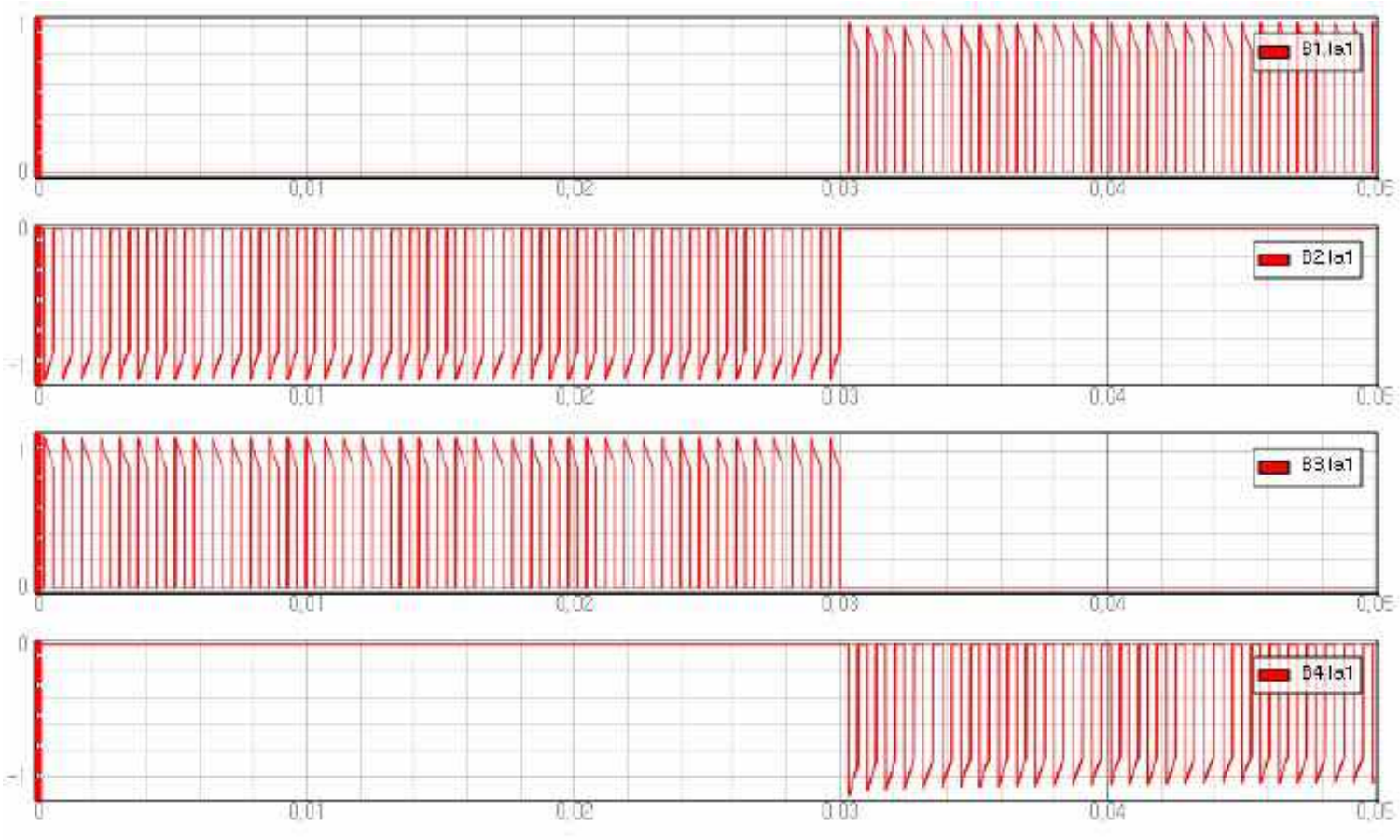
Parameters	Setting		
	IDLE	Charging	Discharging
C	$2048\mu F$		
Duty ratio	$45\% - Deadtime\ \ 5\%$		
Fast f_s	$10kHz$		
Slow f_s	$1kHz$		
R_{loop}	0.15Ω		
Battery module	4S1P module of 18650 cell (3.6V/2.6Ah)		
Initial SOC of Module #1~#4	100, 80, 90, 70%	15, 40, 20, 30%	100, 80, 90, 70%
Operation parameter	$I = 0$	$CC/CV - 4A/16.8V$	$CC - 4A$

- **Real time simulation** is used to assess the performance of **the module equalization for parallel connection.**
- The **cells inside each module** are **regarded as equalized** and **only module equalization is considered**.
- **Initial SOC levels of the modules** are **different in 3 test scenarios**.

4.2 Extended Version of SMC-E for Parallel-connected Modules

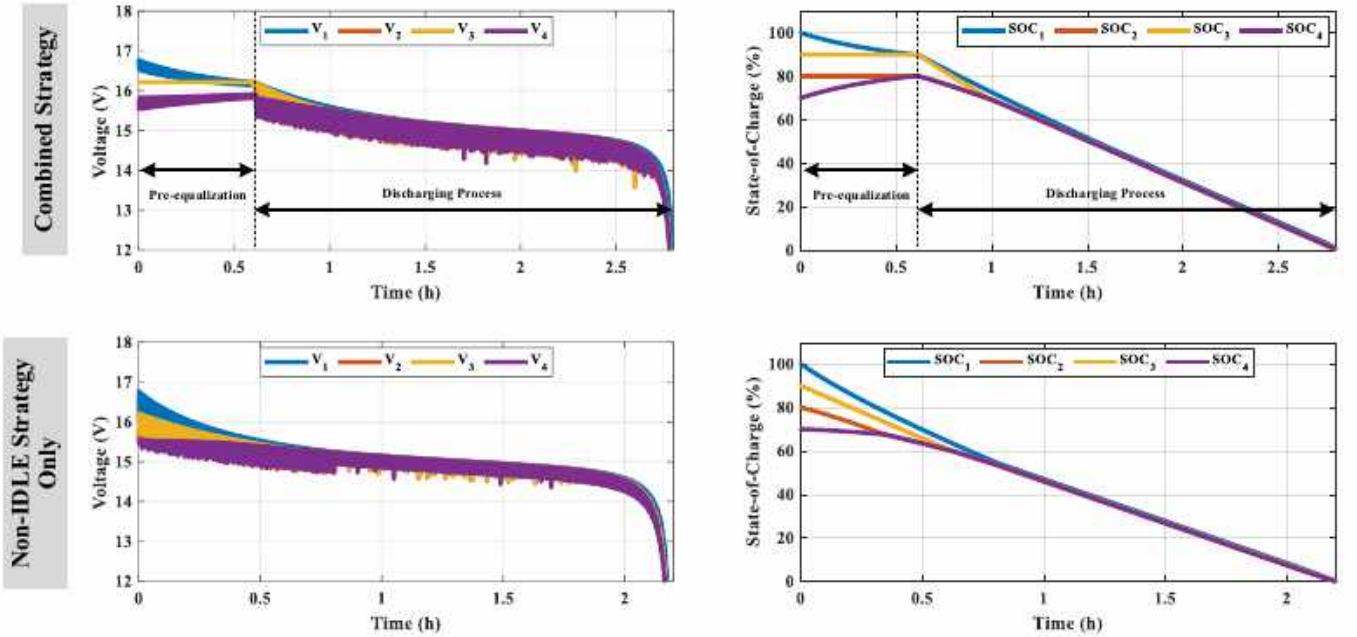


Equalization during IDLE mode

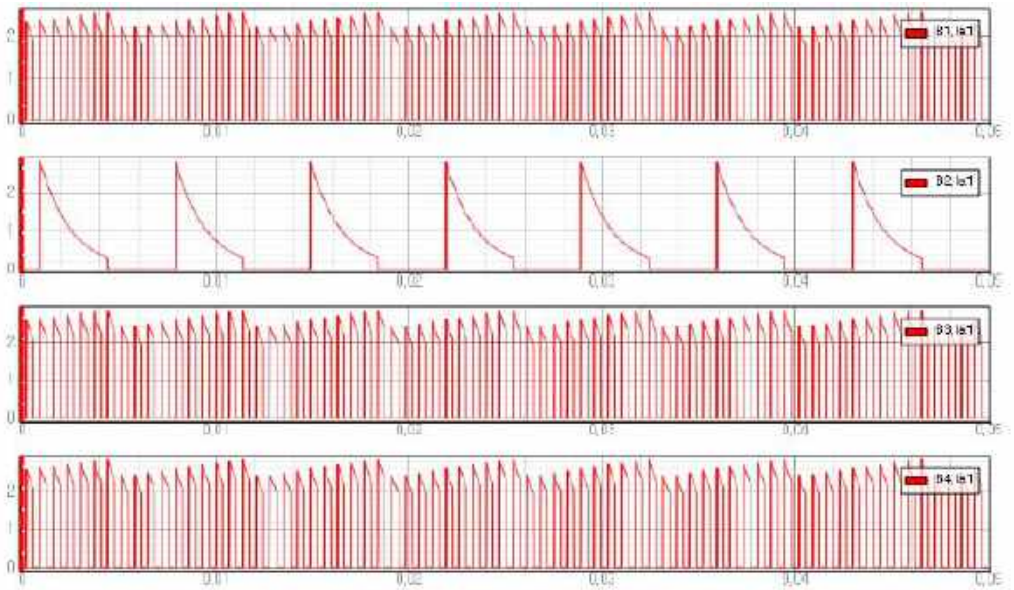


Current waveform of the modules

4.2 Extended Version of SMC-E for Parallel-connected Modules



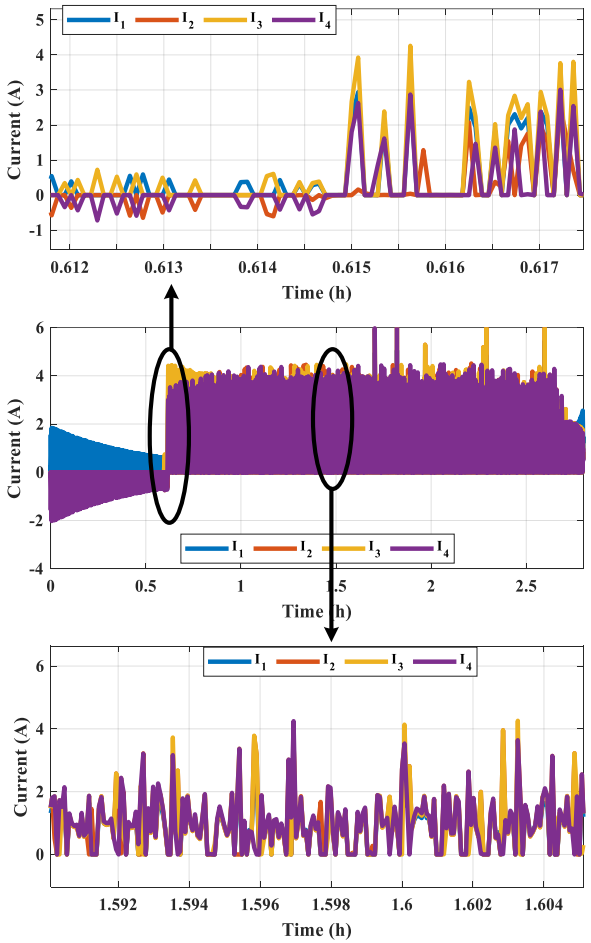
Equalization during Discharging mode



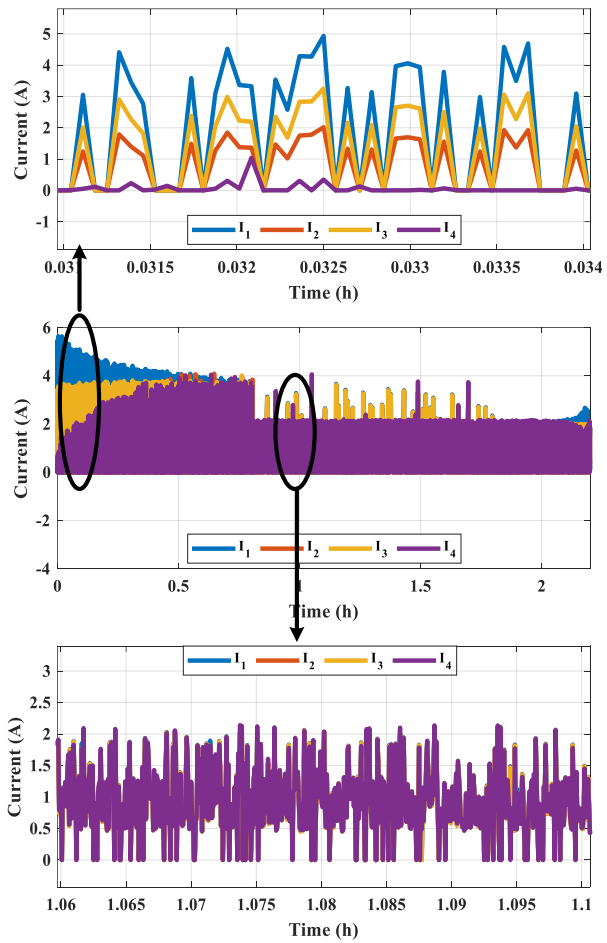
Current waveform of the modules

- **Two strategies are tested:**
  - Modules are equalized in IDLE mode (**pre-equalization process**) before the discharging process is started.
  - Modules are discharged **without pre-equalization process**.

4.2 Extended Version of SMC-E for Parallel-connected Modules



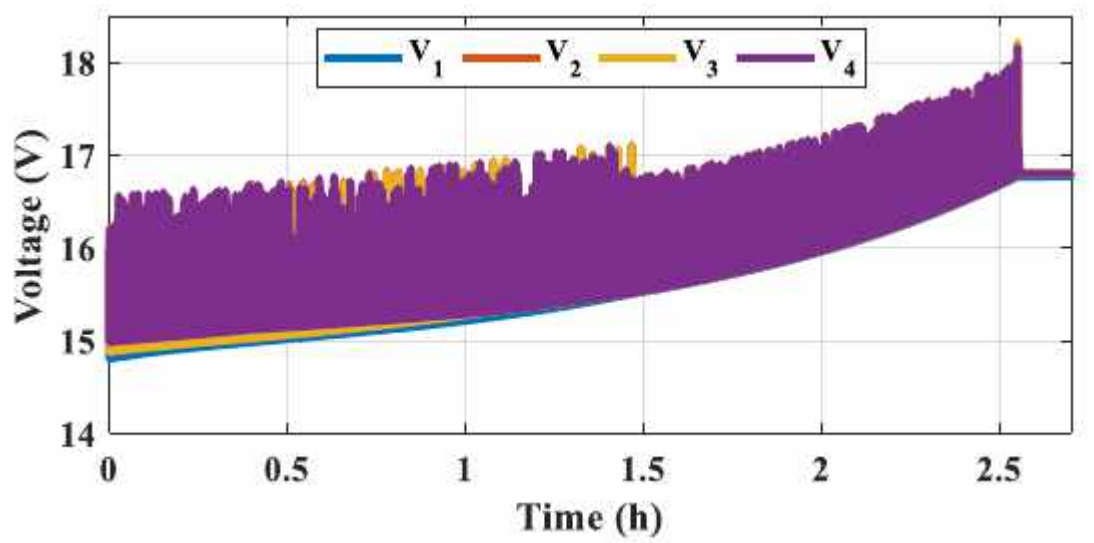
With pre-equ.



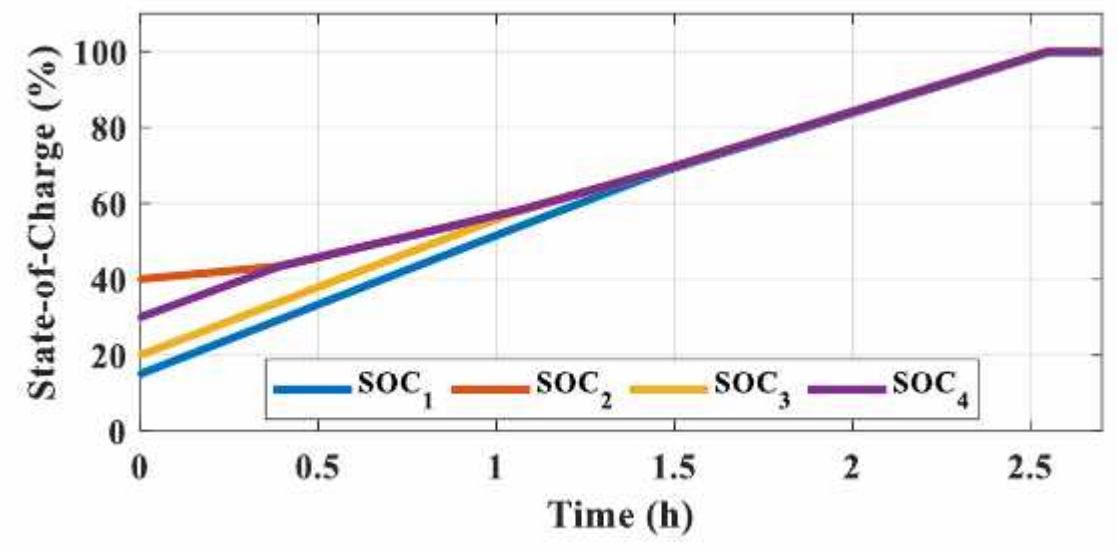
Without pre-equ.

- **Both strategies** can equalize energy level of the modules and regulate the branch current.
- **After the modules are equalized,** load current is distributed evenly.
- **Without the pre-equalization process**, module #1 is discharged by a higher current than the others.
- **With the pre-equalization process**, the inrush current is mitigated.

4.2 Extended Version of SMC-E for Parallel-connected Modules



Voltage Profile during charging mode



SOC Profile during charging mode

- Modules are charged **without the pre-equalization process.**
- **After 1.5h,** the modules are equalized within 1% of SOC difference and they are fully charged at the same time.

4.3 Conclusion of the Chapter

- The extension of the SMC-E for the module equalization strategy is proposed.
- The configuration of equalizer in series and parallel connected modules are almost similar.
- In series connected modules, the hybrid strategy has a 13.5% faster speed than the single SMC-E with optimal pairing algorithm.
- The autonomous strategy in Section 4.1 has a slower speed but the process doesn't require any sensing circuit.
- Two equalization strategies are proposed for the parallel connected modules to achieve a high equalization performance.

Agenda

1. Introduction and Research Motivation
2. Switch-Matrix Capacitor Equalizer for the Cell level
3. Novel Simulation Techniques for Performance Assessment of SET-E in Long-term Operation
4. Module Equalizer System for Series and Parallel Connected Battery Modules
5. Conclusions and Future Works

5. Conclusion

- This thesis has developed multiple strategies for modular battery energy storage systems in order to mitigate the inconsistency in the cell-level and the module-level.
- **The main objectives are achieved:**
  - A novel SMC-E structure is proposed for the cell-level in Chapter 2. An optimal pairing algorithm is proposed to achieve the highest equalization speed without the co-operation of the BMIC circuits. Additionally, the design guidance for the switch-matrix structure, gate driver circuit, and sensing circuit is provided.
  - A unified average model is proposed to accelerate the simulation of the equalizer system over the long term in Chapter 3. Different topological configurations of the equalizer can be assessed and compared within a short time.

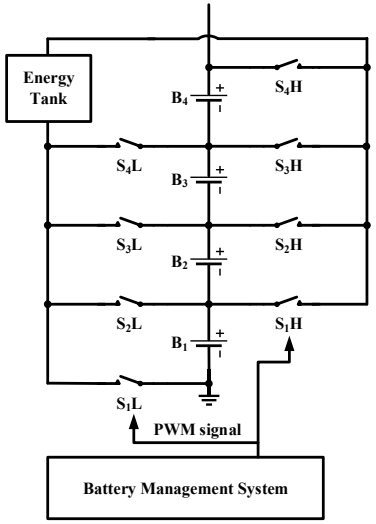
5. Conclusion

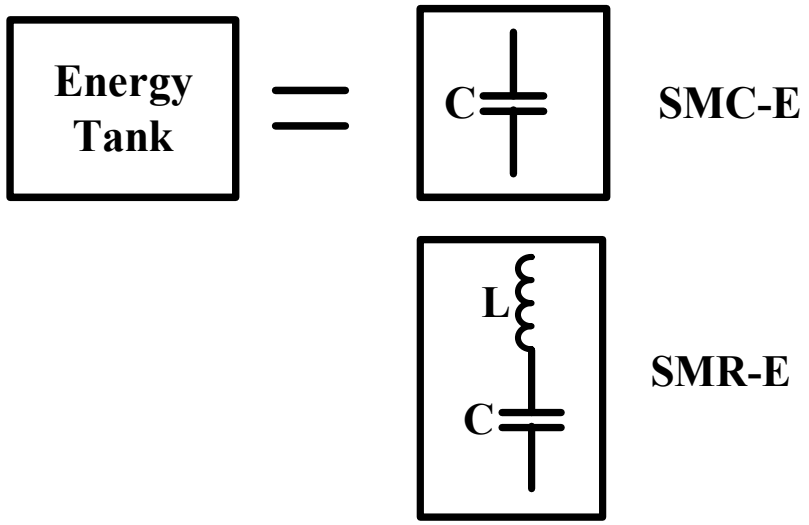
➢ **The main objectives are achieved:**

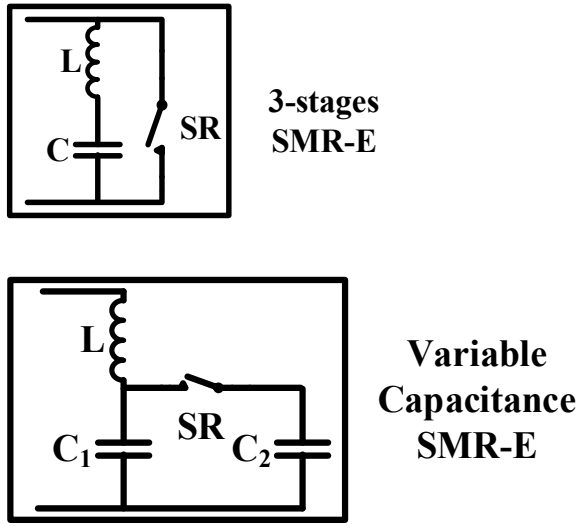
- SMC-E is extended for the module equalizing feature in Chapter 4. Two equalization strategies are introduced to simultaneously achieve the equalization levels I and II. The hybrid strategy shows a high equalization capability for the cells and modules while the autonomous strategy can operated without the guidance of any sensing circuit.
- SMC-E also can be extended for the parallel connected modules. In the IDLE mode, the energy exchange scheme is used to balance the modules. In non-IDLE mode, the branch currents are distributed unevenly to balance the energy level of the modules. Once the equalization condition has been reached, the branch currents are evenly distributed to minimize the loss.

5. Recommendation for the Future Works

- Besides the work that has been done in this thesis, some unexplored subjects may be considered as future studies. The potential topics can be suggested as
  - A family of switch-matrix energy tank equalizer (SMET-E) can be developed from the results of SMC-E. In addition, the other active balancing methods can be combined with the SMC-E to improve the performance of module equalization.







5. Recommendation for the Future Works

- Besides the work that has been done in this thesis, some unexplored subjects may be considered as future studies. The potential topics can be suggested as
  - SMC-E can replace most part of the existing BMIC since it can provide the similar features to the BMIC.
  - The online voltage monitoring and impedance identification for the cells can be integrated into the existing hardware of SMC-E.
  - Under the current distribution scheme, the equalization strategy for the parallel-connected modules has the potential to equalize not only SOC levels but also the SOH levels in the second-life battery modules.

Publications – Journal Papers

1. **Phuong-Ha La** and Sung-Jin Choi. "*Direct Cell-to-Cell Equalizer for Series Battery String Using Switch-Matrix Single-Capacitor Equalizer and Optimal Pairing Algorithm.*" ***IEEE Transactions on Power Electronics* 37**, no. 7 (2022): 8625-8639.
2. **Phuong-Ha La**, and Sung-Jin Choi. 2020. "*Novel Dynamic Resistance Equalizer for Parallel-Connected Battery Configurations*" ***Energies* 13, no. 13: 3315**. https://doi.org/10.3390/en13133315
3. Nguyen-Anh Nguyen, **Phuong-Ha La**, and Sung-Jin Choi. *"Coordinated operation algorithm of pack-chargers and cell-equalizers for SOC adjustment in second-life batteries."* **Journal of Power Electronics 22, no. 1 (2022): 105-115**.
4. Ngoc-Thao Pham, **Phuong-Ha La**, and Sung-Jin Choi, "Online Cell-by-cell SOC/SOH Estimation Method for Battery Module Employing Extended Kalman Filter Algorithm with Aging Effect Consideration," **Journal of Power Electronics (2022)**. https://doi.org/10.1007/s43236-022-00526-7

Publications – Registered Patents

1. KR 10-2367775: Method And Apparatus For Measuring Impedance Of Battery Cell On-Line
2. KR 10-2274812 - Dynamic Resistance Battery Cell Equalization Apparatus For Capacity Optimization Of Parallel Connected Battery
3. KR 10-2463925 - APPARATUS AND METHOD FOR EQUALIZING ENERGY OF PARALLEL-CONNECTED BATTERIES

Publications – International Conference (7 for first author)

1. **Phuong-Ha La**, and Sung-Jin Choi. "*Unified Average Model of Switched-Passive-Network Equalizer for Performance Assessment in Long-term Simulations*." **In 2022 IEEE Transportation Electrification Conference & Expo (ITEC), pp. 1180-1185. IEEE, 2022**.
2. **Phuong-Ha La**, and Sung-Jin Choi. "*Integrated On-line EIS Measurement Scheme Utilizing Flying Capacitor Equalizer for Series Battery String."* **In 2021 IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 975-980. IEEE, 2021.**
3. **Phuong-Ha La**, and Sung-Jin Choi. "*Combined Equalizer Based on Switch-matrix and Bi-directional Converter for Parallel-Connected Battery Packs in Data-Center or Telecommunication*." **In 2021 International Symposium on Electrical and Electronics Engineering (ISEE), pp. 244-248. IEEE, 2021.**
4. **Phuong-Ha La**, and Sung-Jin Choi. "*Reactive Balancing Circuit for Paralleled Battery Modules Employing Dynamic Capacitance Modulation*." **In 2020 IEEE Energy Conversion Congress and Exposition (ECCE), pp. 575-581. IEEE, 2020.**

Publications – International Conference (7/12 for first author)

5. **Phuong-Ha La**, Hong-Hee Lee, and Sung-Jin Choi. "*A single-capacitor equalizer using optimal pairing algorithm for series-connected battery cells.*" **In 2019 IEEE Energy Conversion Congress and Exposition (ECCE), pp. 5078-5083. IEEE, 2019.**

6. **Phuong-Ha La**, Truong Chanh Tin, and Sung-Jin Choi. "*Dynamic Resistance Battery Equalization for Capacity Optimization of Parallel-Connected Cells.*" **In 2019 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019-ECCE Asia), pp. 1-6. IEEE, 2019.**

7. **Phuong-Ha La**, and Sung-Jin Choi. "*Synthesis of balancing topologies for parallel-connected battery cells by principle of duality*." **In 2019 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019-ECCE Asia), pp. 1455-1459. IEEE, 2019.**

8. Nguyen-Anh Nguyen, **Phuong-Ha La**, and Sung-Jin Choi. *"High-speed Target SOC Alignment Algorithm for Second-life Battery Pack Maintenance."* **In 2022 IEEE Transportation Electrification Conference & Expo (ITEC), pp. 131-136. IEEE, 2022.**

Publications – International Conference (7/12 for first author)

9. Ngoc–Thao Pham, **Phuong–Ha La**, and Sung–Jin Choi. *"Online Model-Parameter Identification for Battery Cells Utilizing Switched-Capacitor Equalizers."* **In 2022 IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 01-06. IEEE, 2022.**

10. Nguyen-Anh Nguyen, **Phuong-Ha La**, Ngoc-Thao Pham, and Sung-Jin Choi. "*Novel Battery Equalizer-Charger Symbiosis Structure based on Three-Port DC-DC Converters*." **In 2021 IEEE Energy Conversion Congress and Exposition (ECCE), pp. 180-185. IEEE, 2021.**

11. Truong Chanh Tin, **Phuong-Ha La**, and Sung-Jin Choi. "*A novel asymmetric half-bridge inverter for capacitive wireless power transfer*." **In 2019 International symposium on electrical and electronics engineering (ISEE), pp. 194-198. IEEE, 2019.**

12. Jeong, Chae-ho, **Phuong-Ha La**, Sung-Jin Choi, and Hee-Su Choi. "*A novel target detection algorithm for capacitive power transfer systems*." **In 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 3174-3177. IEEE, 2018.**

Publications – Domestic Conference (5/7 for first author)

1. **Phuong-Ha La** and Sung-Jin Choi, "*Average Modeling of the Switched-Passive-Network Equalizer for Effective Large-scale Battery Simulation*," **KIPE Annual Conference, 2021.**
2. **Phuong-Ha La**, and Sung-Jin Choi. *"Online DCIR Estimation for Series-connected Battery Cells using Matrix-Switched Capacitor Converter.*" **Proceedings of the KIPE Conference. The Korean Institute of Power Electronics, 2020.**
3. **Phuong-Ha La**, and Sung-Jin Choi. *"Optimal Design for Dynamic Resistance Equalization Technique to Minimize Power Loss and Equalization Error."* **Proceedings of the KIPE Conference. The Korean Institute of Power Electronics, 2019.**
4. **Phuong-Ha La**, and Sung-Jin Choi. "*Battery Equalization Method for Parallel-connected Cells Using Dynamic Resistance Technique*." **Proceedings of the KIPE Conference. The Korean Institute of Power Electronics, 2018.**

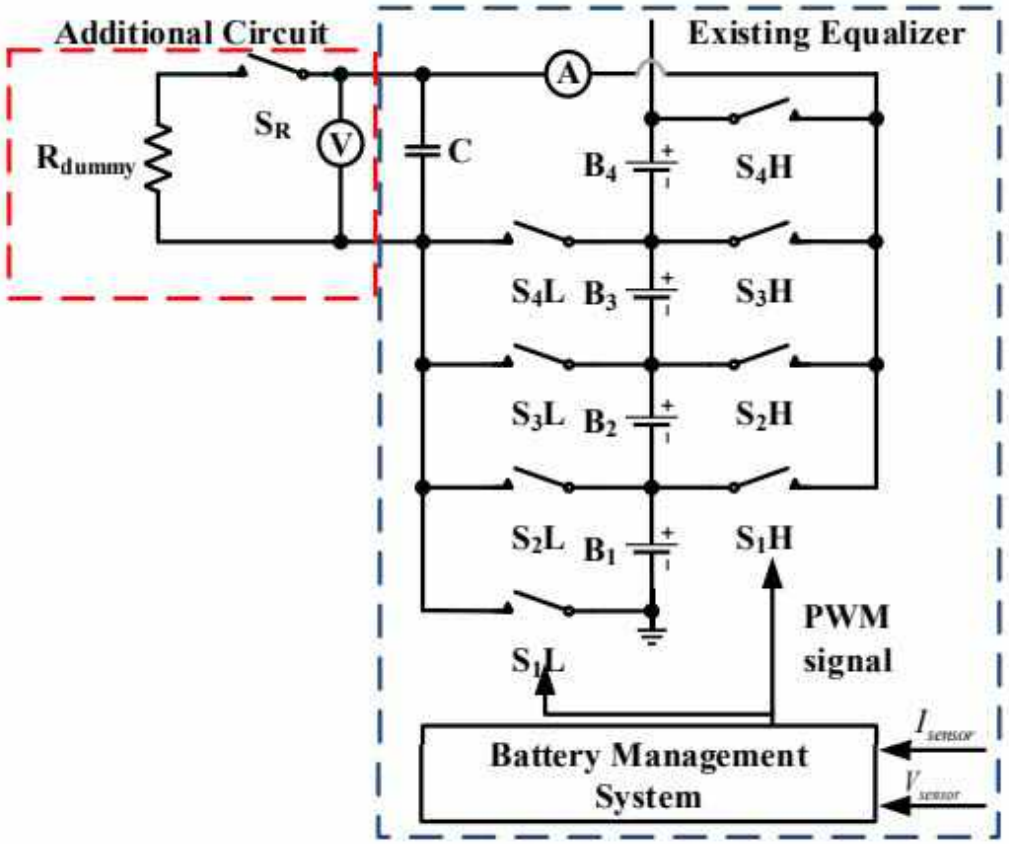
Publications – Domestic Conference (5/7 for first author)

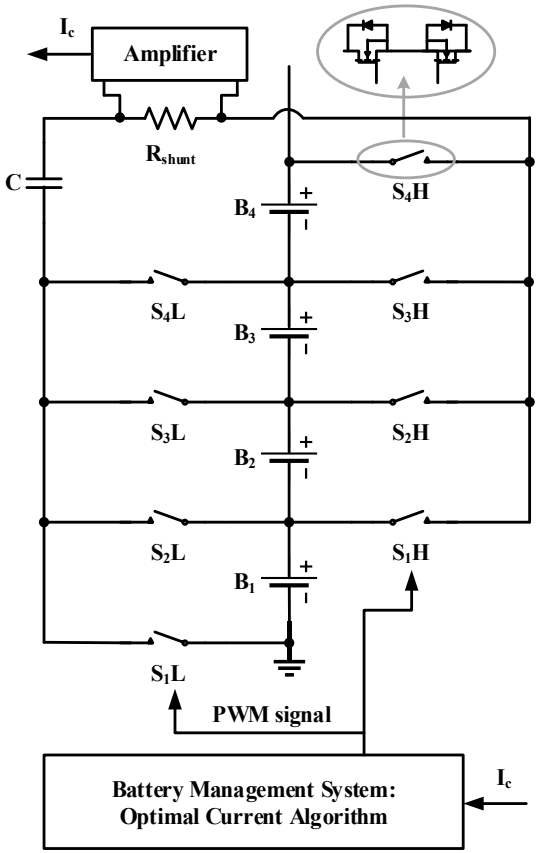
5. **Phuong-Ha La**, Hwi-Yeol Im, and Sung-Jin Choi. "*Development of Low Cost, High-Performance Miniaturized Lithium-ion Battery Tester Using Raspberry Pi Zero*." **Proceedings of the KIPE Conference. The Korean Institute of Power Electronics, 2017.**
6. Nguyen-Anh Nguyen, **Phuong-Ha La**, and Sung-Jin Choi. *"High-Speed Battery SOC Adjustment Algorithm utilizing Bi-directional Cell Balancers in Coordination with Pack Charger."* **KIPE Annual Conference (2021): 119-120.**
7. Ngoc-Thao Pham, **Phuong-Ha La**, and Sung-Jin Choi. "*Comparison of Different Current Sampling Strategies for an Online Battery Model Identification using Switched-Capacitor Equalizer."* **KIPE Annual Conference (2021): 117-118.**

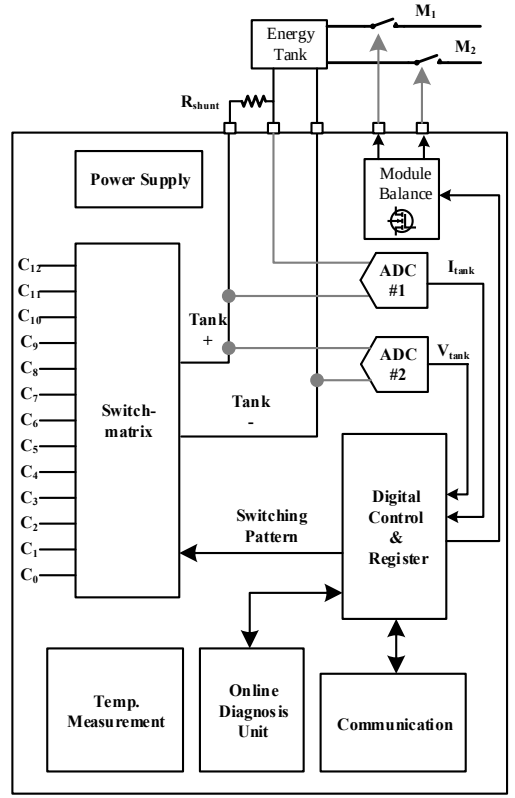
Thank You

for Your Attendance!

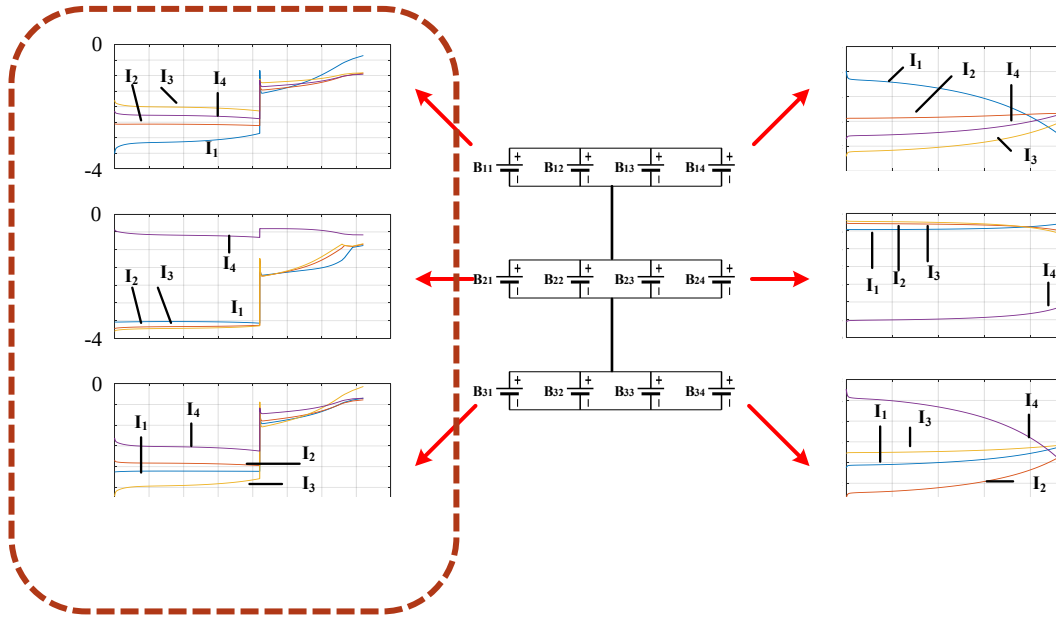
5. Recommendation for the Future Works



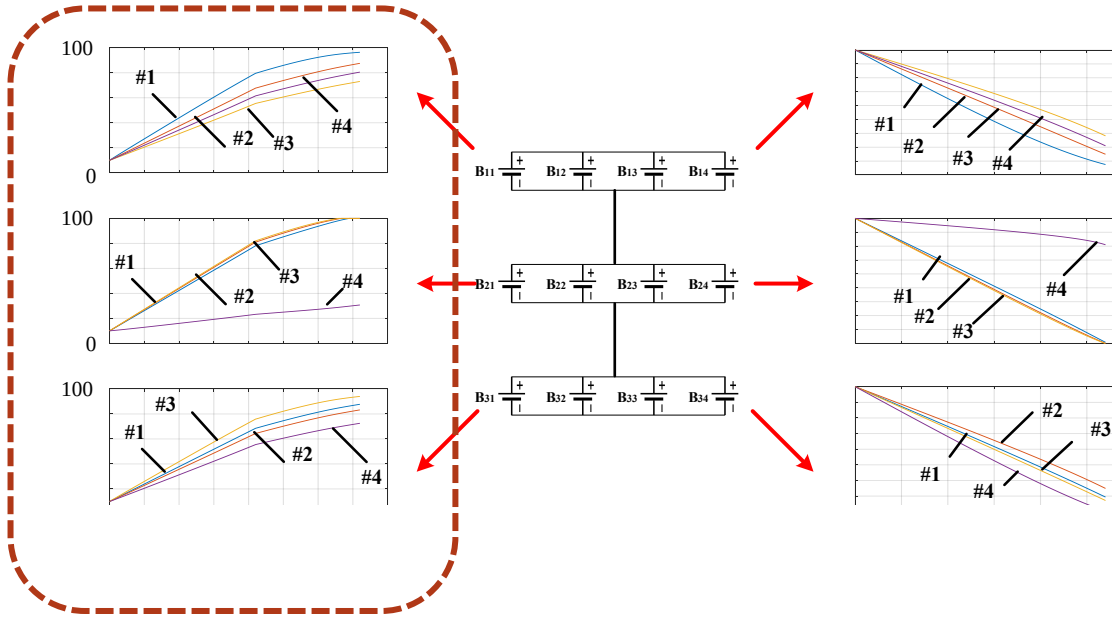




1.5 Impact of the Cell-inconsistency



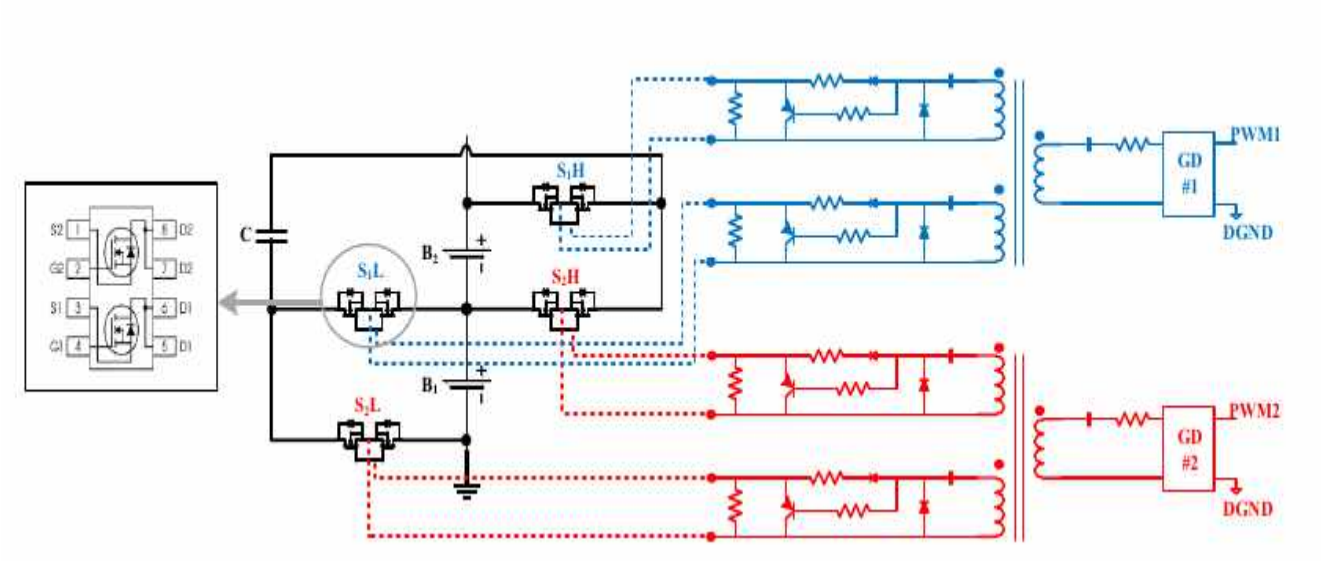
Uneven current distribution

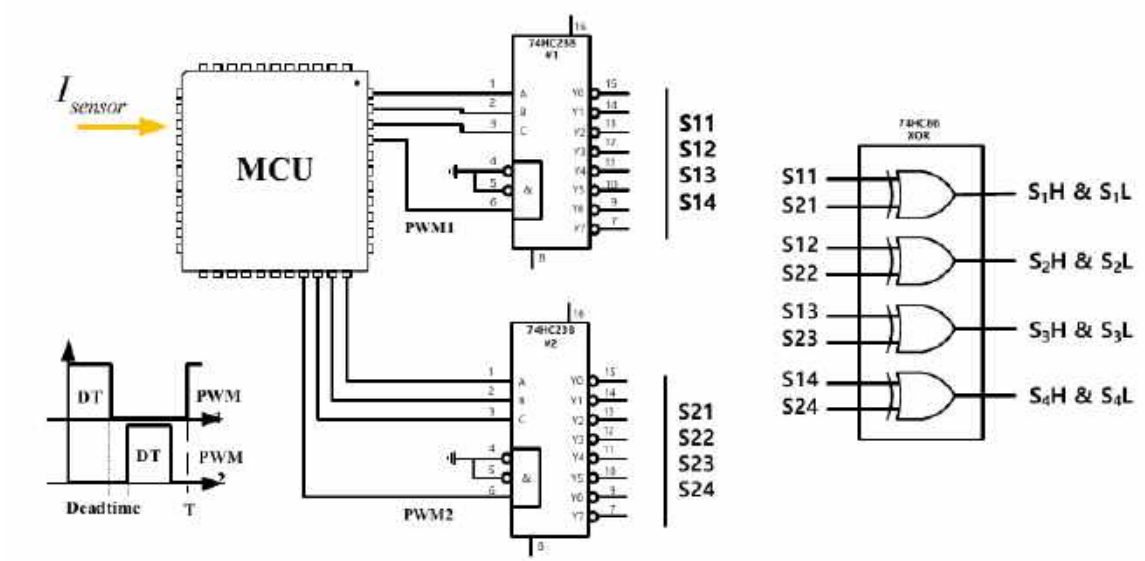


Process is stopped before every cells are fully charged or discharged

- Assess the **cells performance in 3S4P** battery system, which have **different impedance and capacity**.
- **Cell-inconsistency occurred** in both **series and parallel connection**.
- **Uneven current distribution** between the branches in **parallel connection** is more serious.

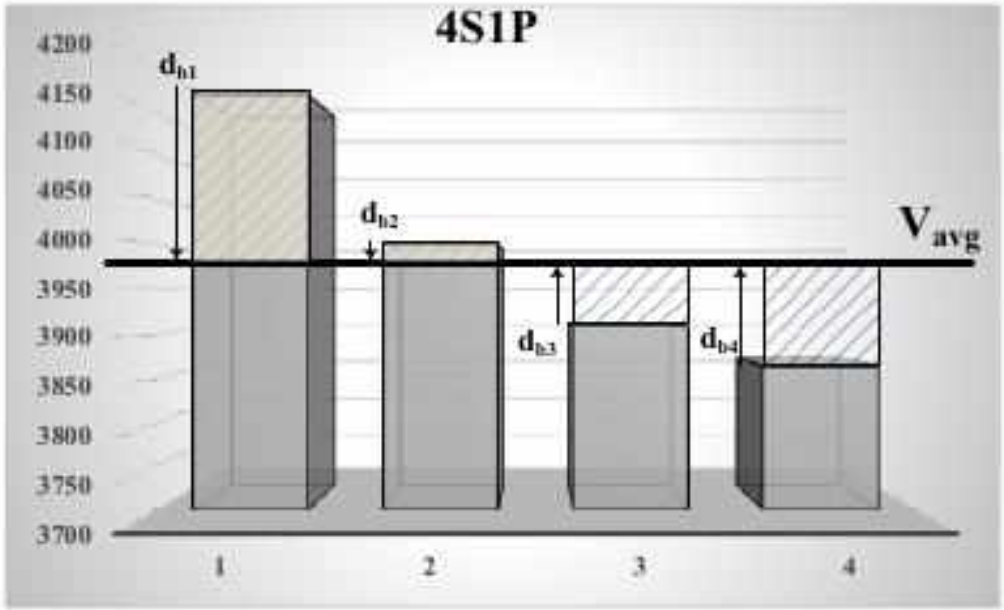
2.3 SMC-E: Design Consideration – Gate Driver

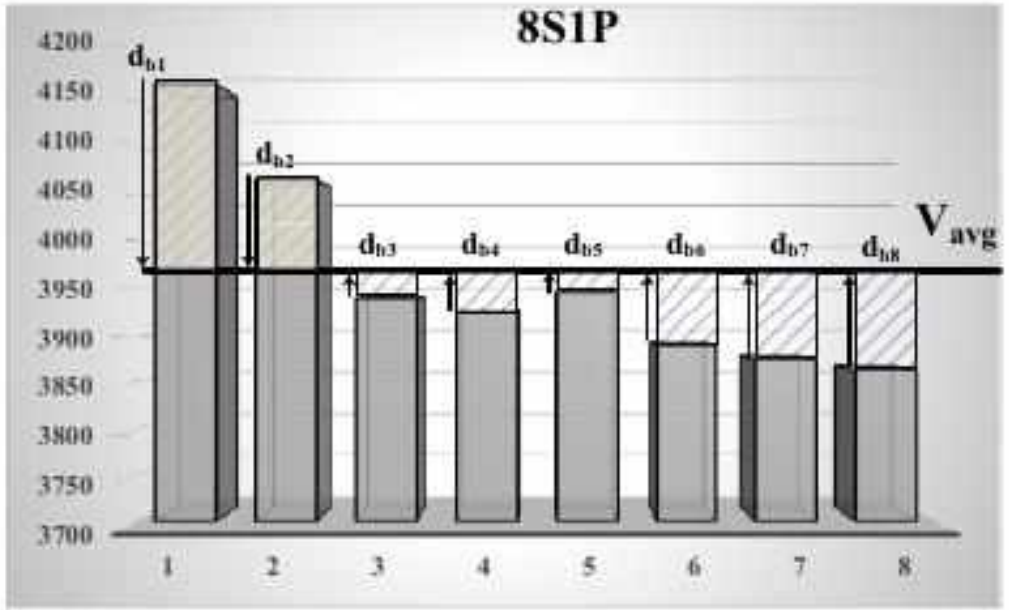




- **On-semiconductor NVMFD5485NL dual N-channel** form a **bi-directional switch**, which consists of **two back-to-back MOSFETs**.
- The **switches S_kH and S_kL** are controlled by a **1:1:1 pulse transformer gate driving circuit.**
- Analog circuits are used to **extend the PWM signal from MCU**.

4.1 Extended Version of SMC-E for Series-connected Modules





- Although the **voltage deviation is similar**, the **moved energy after equalization process in 2 cases are different.**

$$V_{avg} = \frac{1}{N}\sum_{n=1}^{N} V_{bk},$$

$$d_{bk} = V_{bk\_init} - V_{bk\_after},$$

$$d_{total\_\#m} = \sum_{n=1}^{N} |d_{bk}|,$$

4.1 Extended Version of SMC-E for Series-connected Modules

Table 4.1 VOLTAGE LEVELS OF THE CELLS (mV)

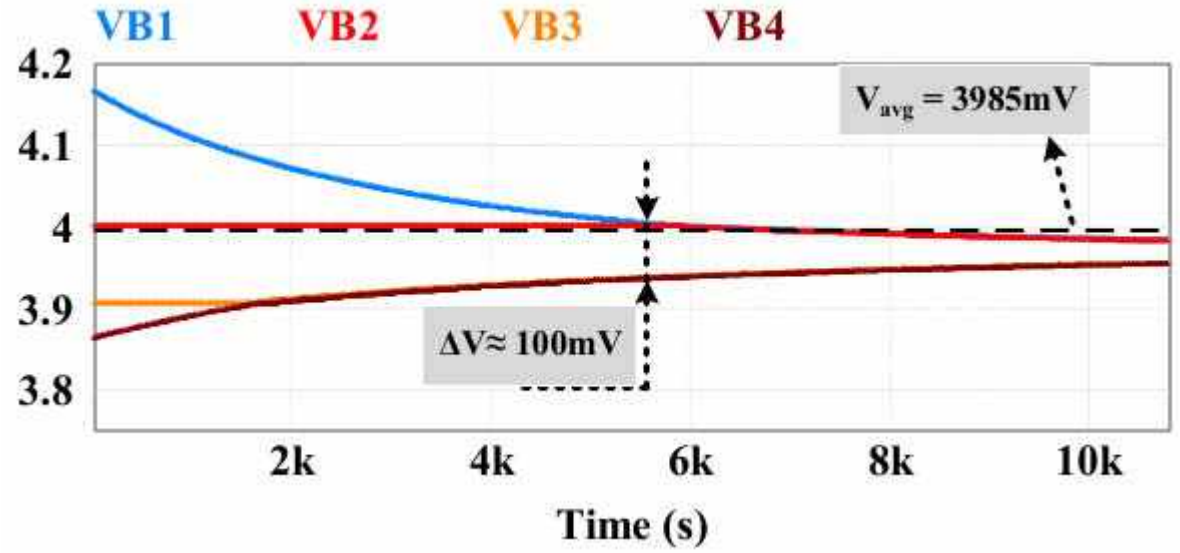
	Cell #1	Cell #2	Cell #3	Cell #4	Cell #5	Cell #6	Cell #7	Cell #8	V_{avg}	ΔV
Initial #1	4170	4000	3907.6	3863.7	-	-	-	-	3985.33	306.3
Exp. #1	4008	4000	3967	3967	-	-	-	-	3985.5	41
d_{bk} **in #1**	162	0	−59.4	−103.3	-	-	-	-	–	–
Initial #2	4170	4066	3940	3926	3947	3890	3875	3863.7	3959.71	306.3
d_{bk} **in #2**	210.288	106.288	−19.72	−33.72	−12.7125	−69.72	−84.7125	−96.0125	–	–

- A higher total moved energy requires a longer equalization time.

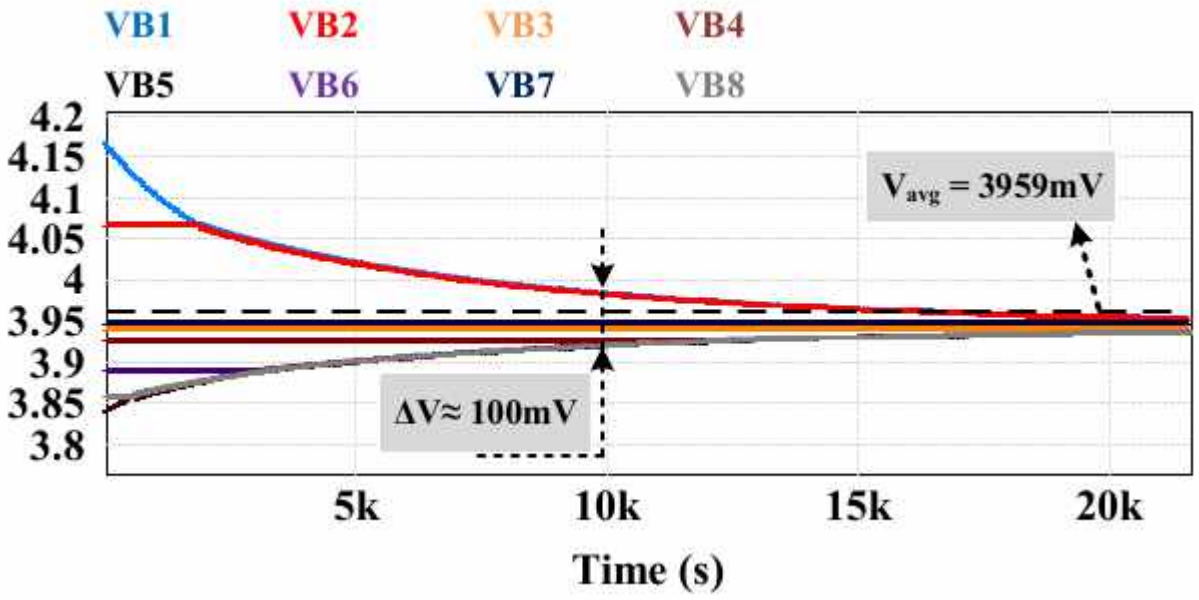
$$\frac{d_{total\_\#1}}{t_1} = \frac{d_{total\_\#2}}{t_2}$$

$$t_2 = \frac{d_{total\_\#2}}{d_{total\_\#1}} t_1.$$

4.1 Extended Version of SMC-E for Series-connected Modules



4S1P String



8S1P String

- A higher total moved energy requires a longer equalization time.

Battery Configuration in EV and BESS

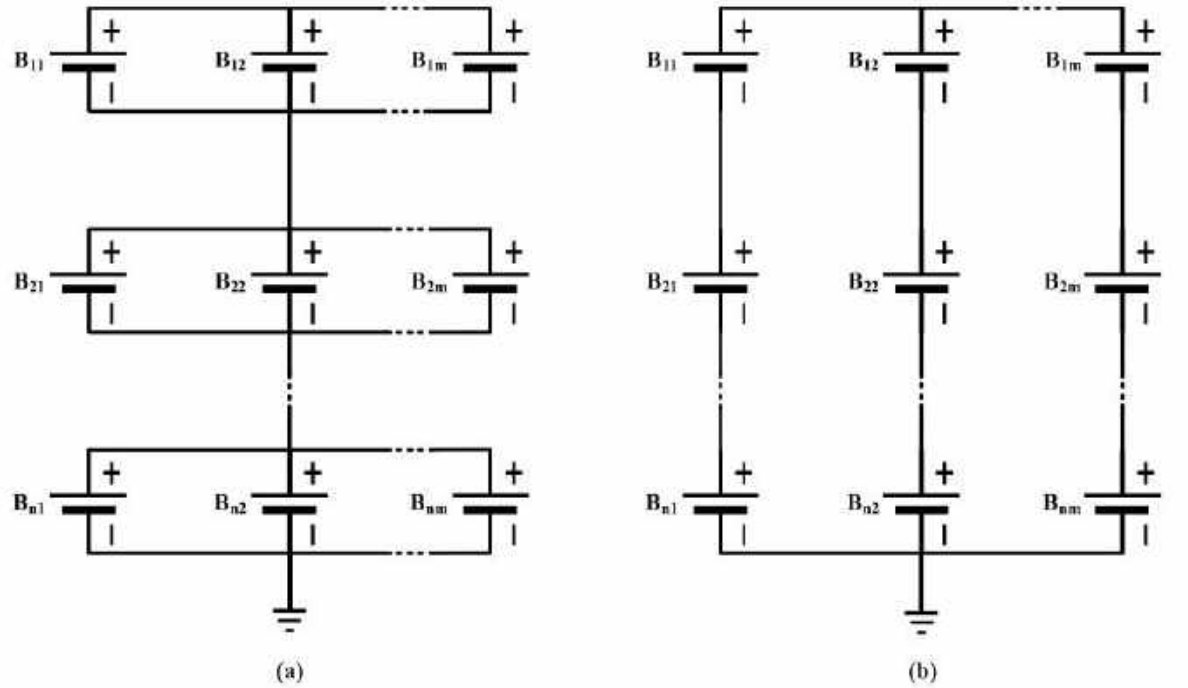


Fig. 1.1 Battery configuration in ESS: (a) nSmP configuration; (b) nPmS configuration.

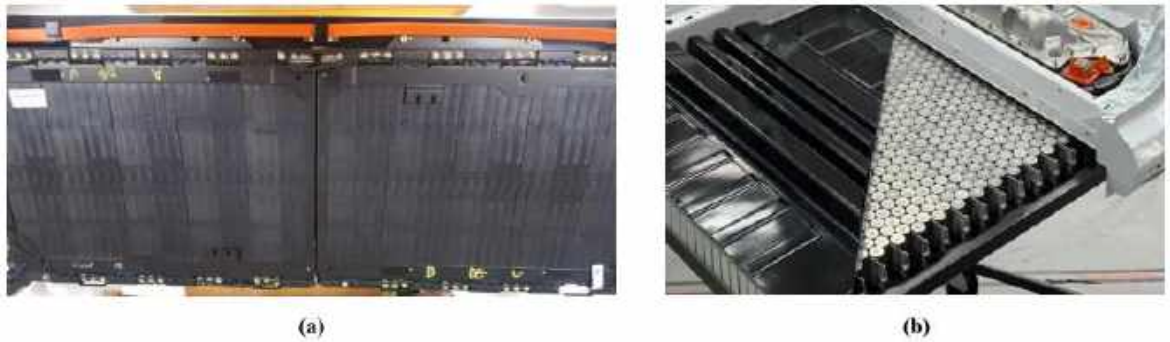
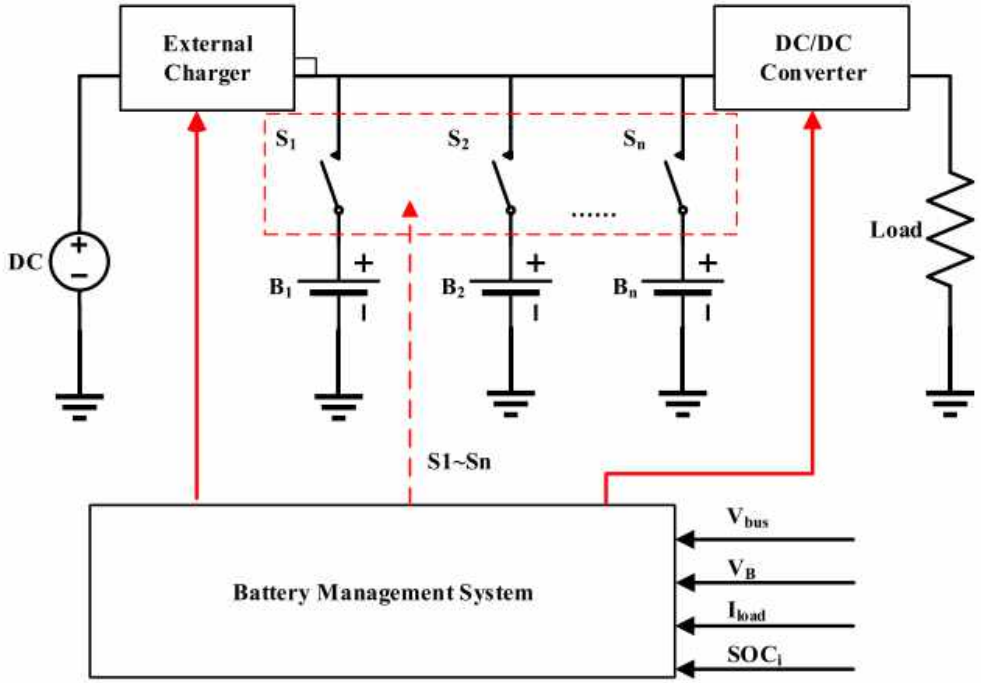


Fig. 1.2 Example of cell configuration in EV: (a) Pouch type; (b) Cylindrical type.

Battery Configuration in Telecom. and Data-center



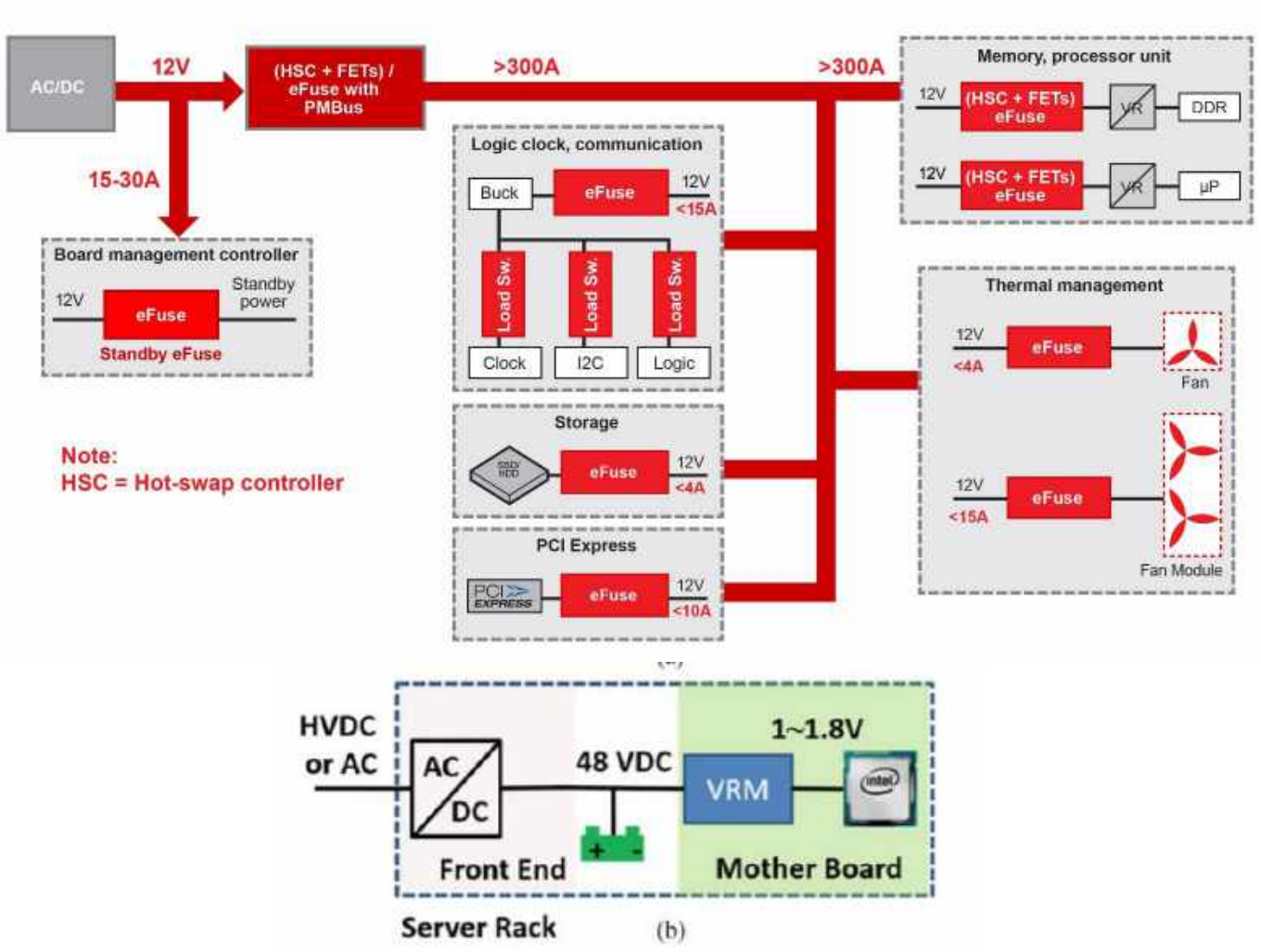


Fig. 1.3 Battery configuration in telecom. and datacenter application.

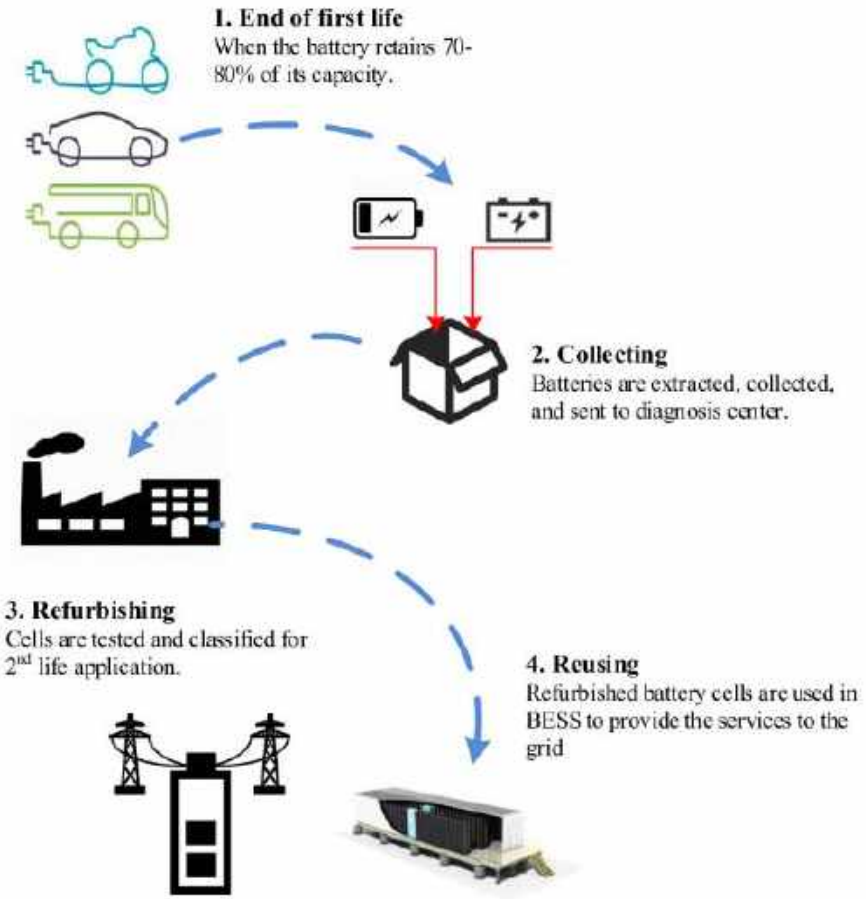


Fig. 1.4 Life cycle and seconds-life battery concept.

Second-life Battery Application

- Battery Pack of EV must be replaced when the SOH is lower than 80%.
- We can re-use the retired battery pack for the BESS application, which is called second-life battery application.
- SL-BESS is a good candidate for the grid-tiered power system or renewable energy system.

Aging Pattern and the Cell-Inconsistency Probability

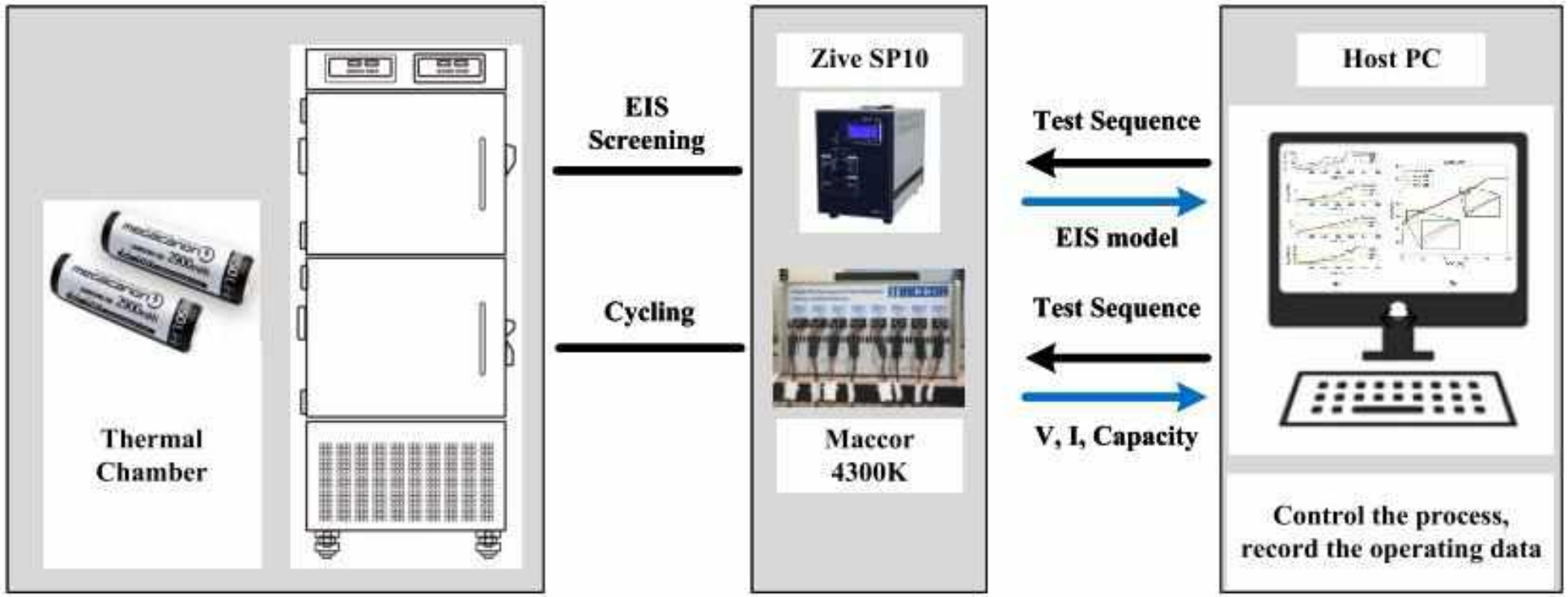


Fig. 1.7 Experimental setup for the aging assessment.

Modularized Structure of the BMS

Table 2.1 COMPARISON OF BMIC FEATURE.

Manufacturer	Model	No. of Channel	Balancing	Communication	Measuring error	Temp. sensing channel
AD	**LTC6804**	12	Passive	Daisy Chain Iso-SPI	1.2mV	2
AD	**LTC6811**	12	Passive & Active	Daisy Chain Iso-SPI	1.2mV	2
Infineon	**LLE9012DQU**	12	Passive	Iso-UART	78mV	5
ST	**L996963E**	14	Passive	Iso-UART	2mV	7
TI	**bq76PL455A-Q1**	16	Passive & Active	Iso-UART	3mV	8
MAX	**MAX17823B**	12	Passive	Daisy Chain Iso-UART	5mV	2

Equalizer Classification

Table 2.2 CLASSIFICATION OF BATTERY EQUALIZERS

Ref.	Structure	Equalization Scheme	Target Objects	Control Technique
[61],[34]	Switched Resistor	Dissipative	Individual cell	Governed
[29]	Shunt MOSFET	Dissipative	Individual cell	Governed
[15]	Multiple Converters	Regenerative	Individual cell	Governed
[19]	Switch-matrix and Converter	Regenerative	Direct pack to cell	Governed
[33],[36], [13]	Multi-winding or Multiple Transformer	Regenerative	Any-cell to any-cell	Autonomous
[28], [47]	Switched Inductor	Regenerative	Adjacent cells	Autonomous
[65]	Switch-matrix and Inductor	Regenerative	Direct any-cell to any-cell	Governed
[46]	Switched Capacitor-Classical Structure	Regenerative	Adjacent cells	Autonomous
[4]	Switched Capacitor-Double-tiered Structure	Regenerative	Adjacent cells	Autonomous
[27]	Switched Capacitor-Chain Structure	Regenerative	Adjacent cells	Autonomous
[57]	Switched Capacitor-Star Structure	Regenerative	Any-cell to any-cell	Autonomous
[63]	Switched Capacitor-Reconfiguration	Regenerative	Adjacent cells	Autonomous
[66], [38], [58]	Switched Resonance Structure	Regenerative	Any-cell to any-cell	Autonomous

Equalizer Classification – Active Methods

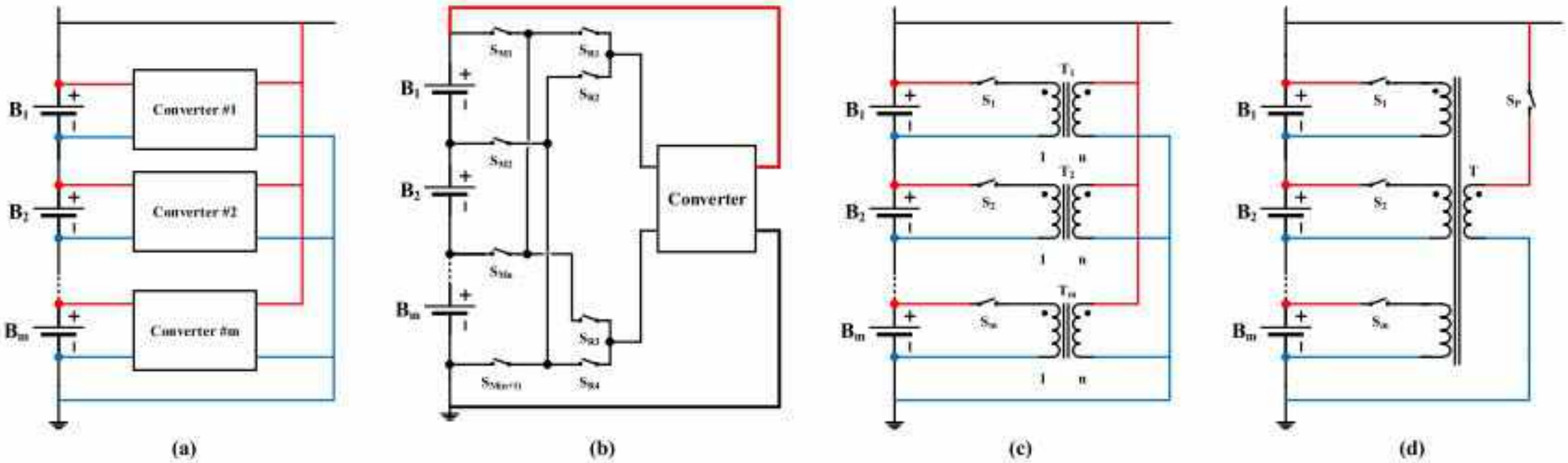
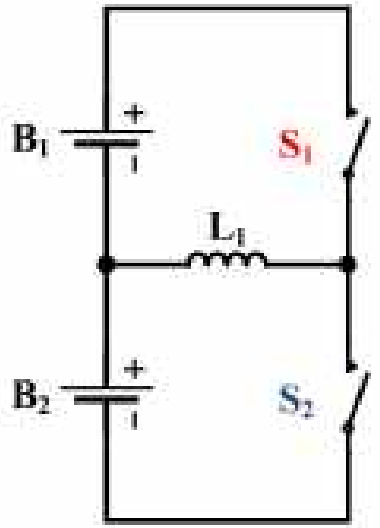
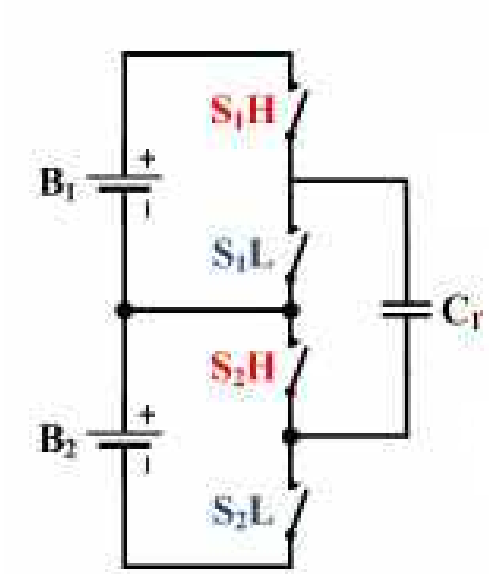


Fig. 2.3 Energy regenerative scheme group - Converter & Transformer type: (a) Individual converter; (b) Switch-matrix converter; (c) Individual transformer; (d) Multi-winding transformer.

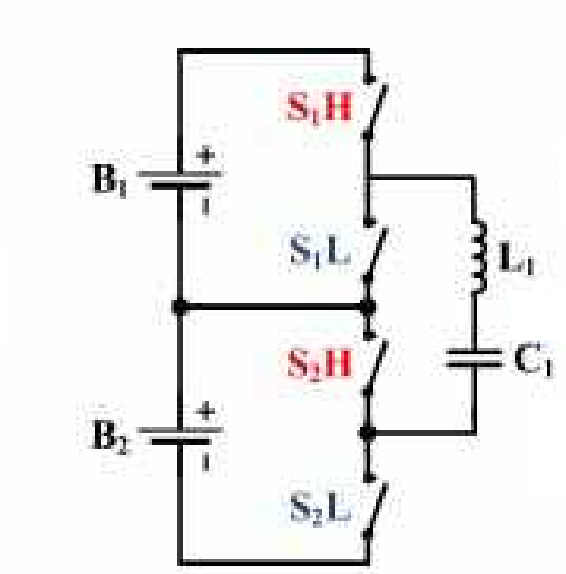
Topology Evolution – UA model for Long-term Simulation



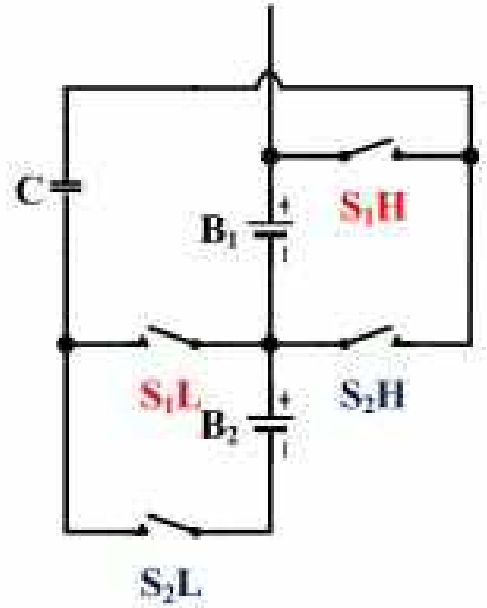
SI-E



SC-E



SR-E



SMSC-E

- Switched-energy-tank equalizers (SET-Es) show superiority than the other methods in terms of simplicity, volume, and cost.
- The common topology configurations adopt autonomous and governed control strategy.

Use Case Application for Equalizer Design

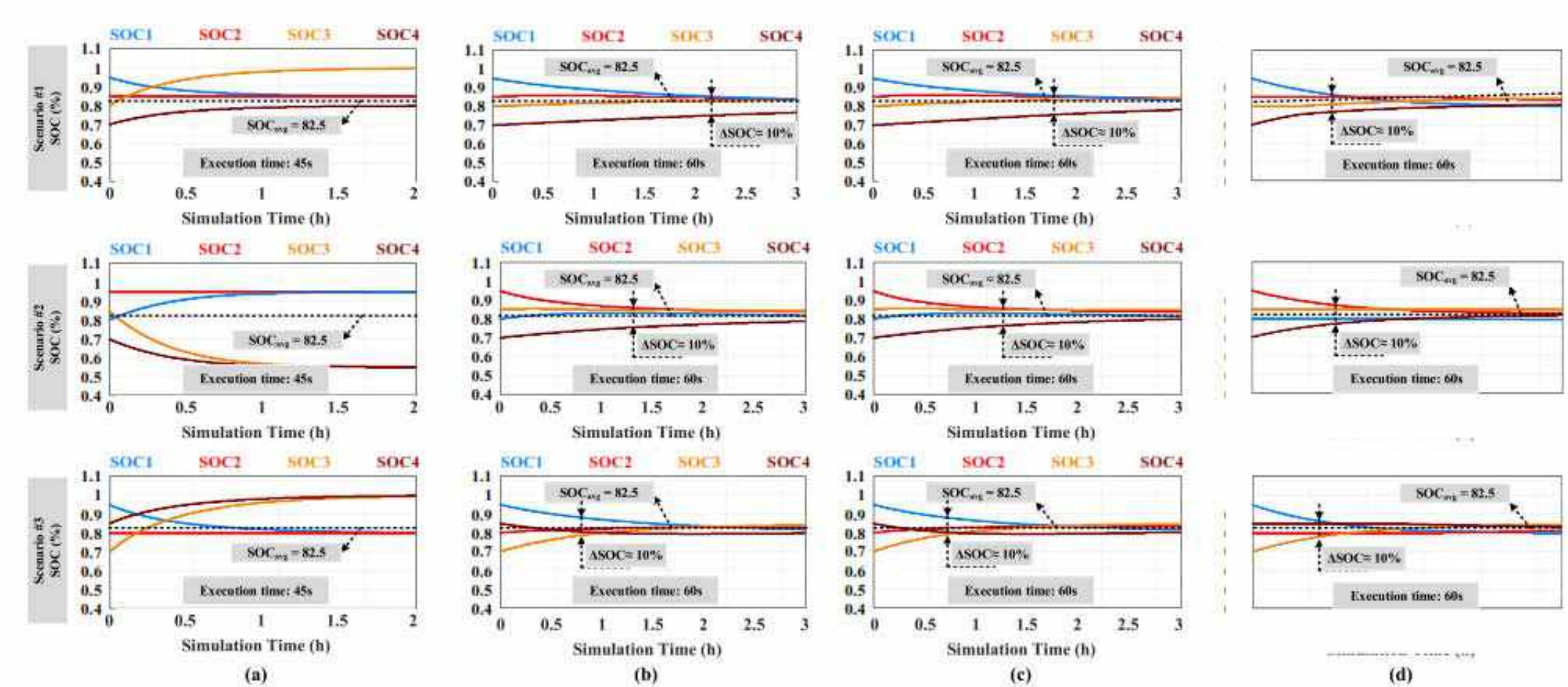


FIGURE 11: SOC profiles of the cells by: (a) SI-E; (b) SC-E; (c) SR-E; (d) SMSC-E.

Use Case Application for Equalizer Design

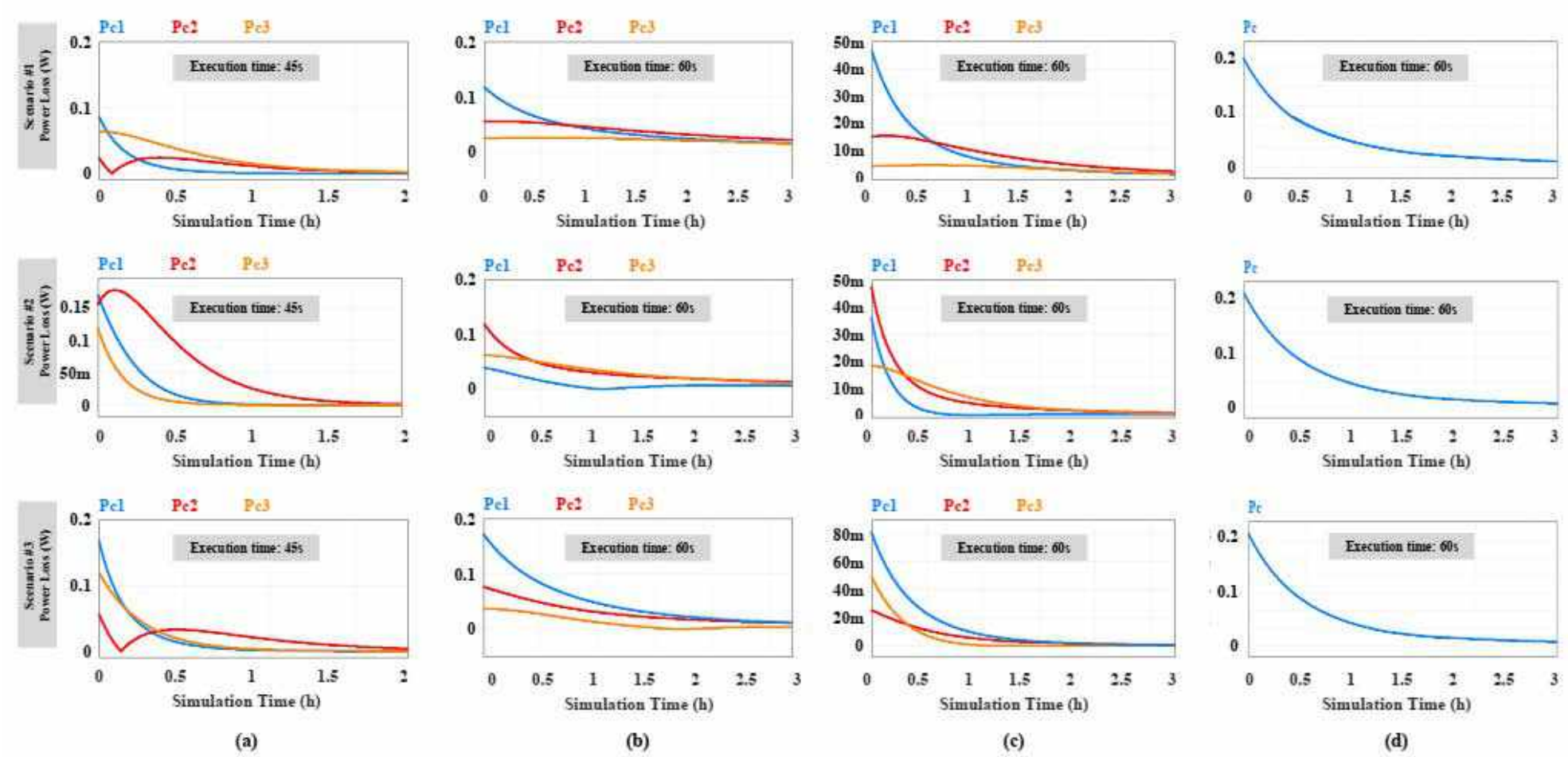
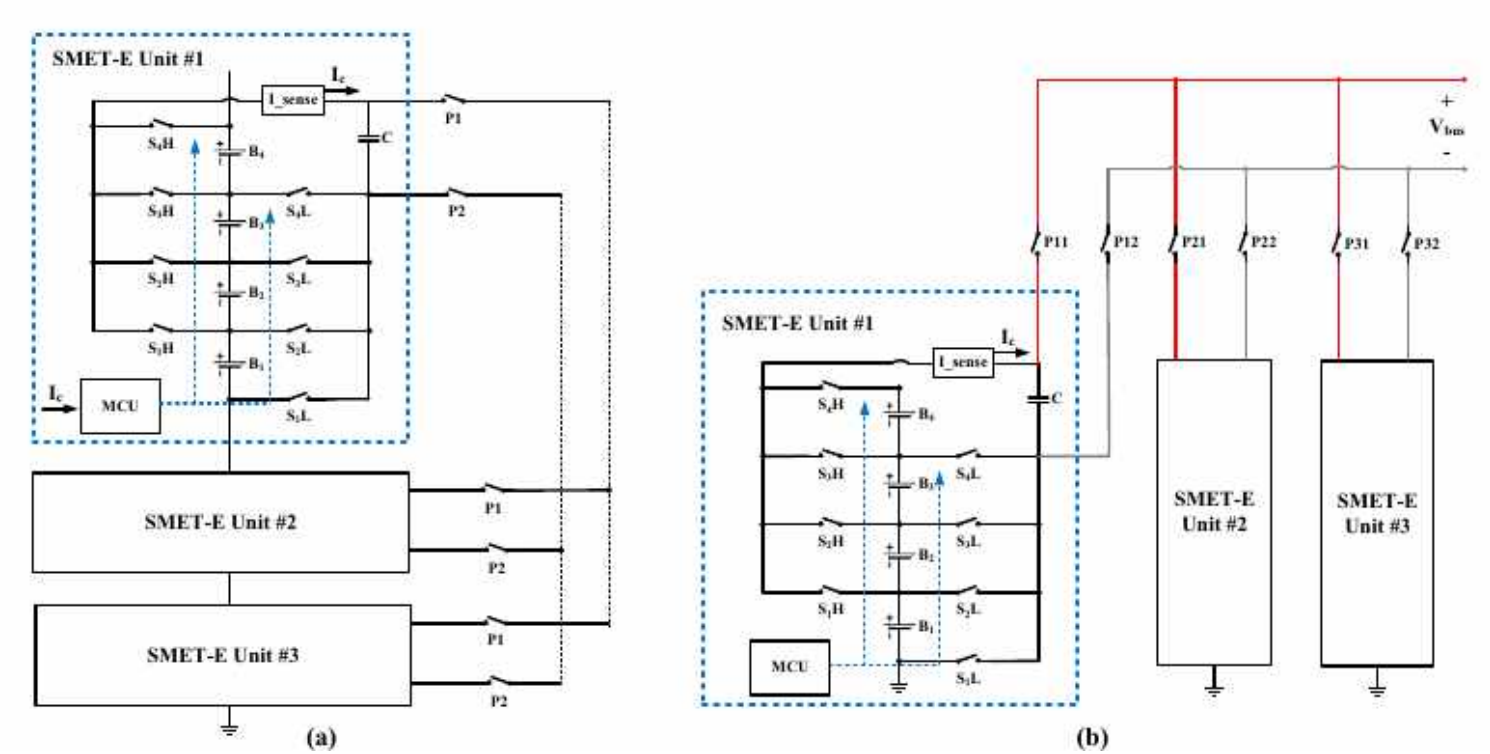


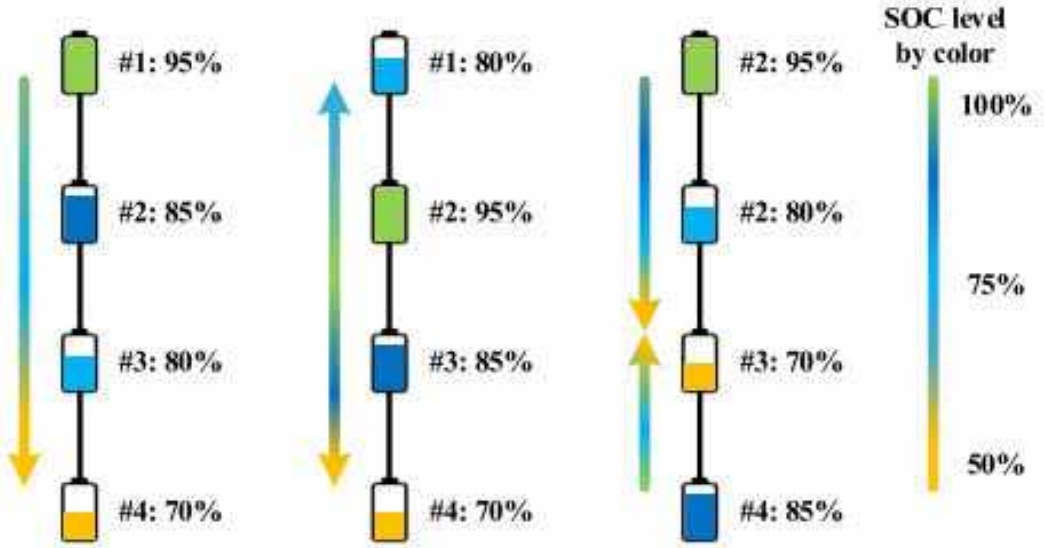
FIGURE 12: Power loss profiles of the cells by: (a) SI-E; (b) SC-E; (c) SR-E; (d) SMSC-E.

Modular Structure of Equalizer



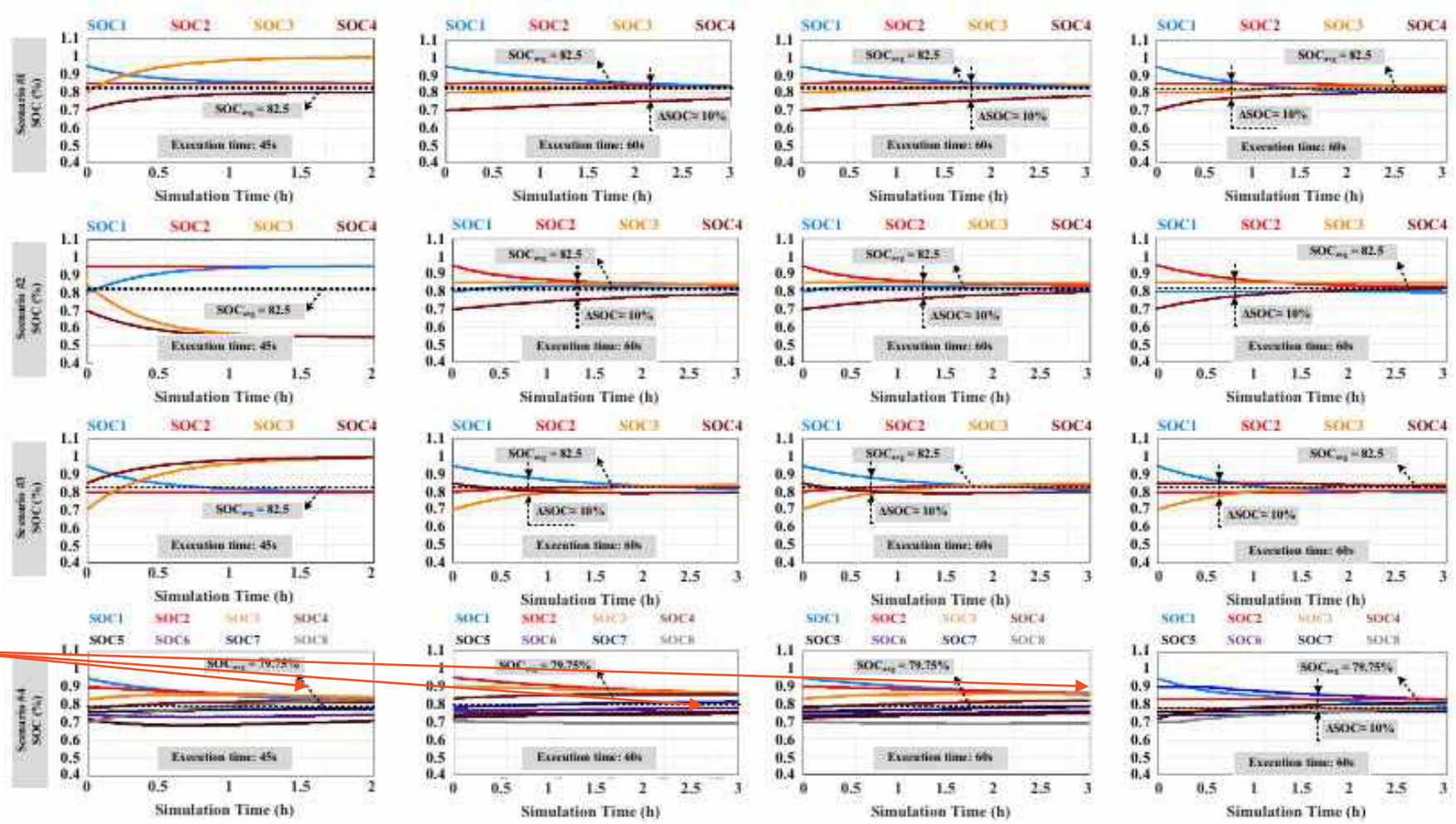
- The modular equalization system is divided into multiple SMET-E units.
- Two additional switches are added to the SMET-E unit for modular equalization.
- When P1 and P2 are on, the energy tanks of the SMET-E units are connected in parallel

Use Case Application for Equalizer Design



- Equalizers must be tested under various scenarios of initial energy distribution to assess the performance stability.
- Various evaluation criteria are considered during the development of a equalizer.

3.2 UA-Model Based Simulation – Performance Assessment



SI-E SC-E SR-E SMC-E

Performance is reduced.

Influence of the cell number exists, but it is less than that of the other equalizers.